XIX IMEKO World Congress
Fundamental and Applied Metrology
September 6–11, 2009, Lisbon, Portugal

IMPLEMENTATION OF HIGH RESOLUTION DAC TEST STATION: A CONTRIBUTION TO DRAFT STANDARD IEEE P1658

Aldo Baccigalupi [1], *Mauro D'Arco* [2], *Annalisa Liccardo* [2], *Michele Vadursi* [3]

[1] Dipartimento di Informatica e Sistemistica, Università degli Studi di Napoli Federico II, Napoli, Italy, baccigal@unina.it
[2] Dipartimento di Ingegneria Elettrica, Università degli Studi di Napoli Federico II, Napoli, Italy, {darco; aliccard}@unina.it
[3] Dipartimento per le Tecnologie, Università degli Studi di Napoli "Parthenope", Napoli, Italy, vadursi@uniparthenope.it

Abstract – The paper deals with the implementation of a measurement station for the test of high resolution of Digital-to-Analog Converters (DACs). The basic idea relies on the employment of a differential amplifier that provides a signal related to the difference between the voltage generated by the DAC under test and a reference signal. To solve problems associated to synchronization, the reference signal is gained by treating the DAC output voltage through a narrow band filter. Thanks to the differential amplifier, the difference signal, which holds information about DAC non linearity, is hugely expanded and, thus, can be acquired by means of an Analog-to-Digital converter whose resolution is lower than that of the DAC under test.

Keywords: Digital-to-Analog converter, Filters, Differential amplifier.

1. INTRODUCTION

The characterization of high resolution Digital-to-Analog converters is a challenge nowadays still open. The static characterization could be, in theory, fulfilled by means of high accuracy voltmeters even though the test duration [1-4] makes it not practicable. But, still more challenging is high resolution DAC dynamic characterization. In this case, the use of a high speed/high resolution reference ADC (Analog to Digital Converter), able to gather the DAC variable voltage, should be required. But, present technological bound can produce DACs which exhibit resolution much greater then ADCs [5].

Consequently, at present, a Standard or a set of recommendations defining specific practices for the estimation of synthetic parameters able to quantify the DAC quality, does not exist. Many researchers are currently working for drawing up specific procedures and, some of them, are also employed in manufacturing societies.

The proposals available in literature show very interesting features, but in these papers the problems arising when the proposed methods are experimentally implemented are not taken into account. Indeed, the results reported in the recent literature are obtained only through numerical simulations and it confirms how far the definition of a standard procedure suitable for actual tests is.

In this work, the authors pay particular attention to the put into operation feature. After a brief description of the proposed characterization method, in fact, the attention is mainly focused on the realization of the experimental setup. In particular, a variety of practical difficulties and the solutions proposed to preserve measurement resolution and accuracy are pointed out. The research activity aims at providing some guide lines for the implementation of a test station for DAC characterization, which could be straightforwardly repeatable.

2. ANALYSIS OF PRESENT-DAY PROPOSALS

Some of the solutions present-day proposed in scientific literature to characterize high resolution DACs suggest to add a constant voltage, whose amplitude is lower than the DAC LSB, to a sinusoidal signal generated by the DAC under test [6-7]. The constant voltage is regularly adapted in such a way that the produced output overcomes the transition threshold of the reference ADC. The main drawback associated with this approach is the use of an adder circuit because it is necessary to take into account the effects of both the offset voltage introduced by the adder and the uncertainty of the passive network used in the circuit. The latter consideration, particularly holds for the adopted resistors, since the voltage values applied across them are extremely different from each other (DAC output and constant voltage). Obviously, the aforementioned uncertainties should be limited to values lower than DAC LSB in order to reliably characterize the DAC performance.

An attractive proposal is given in [8], even though it refers to a static characterization conducted through the measurement station shown in Fig.1. The basic idea underlying the proposal consists in using a low-resolution

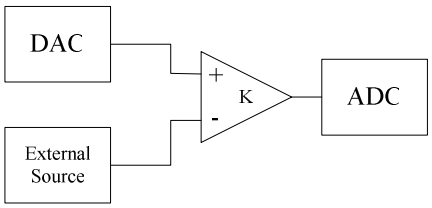

Fig. 1. Scheme of the proposal in [8] for dynamic characterization of DACs.

reference ADC to digitize the difference between the voltage generated by the DAC and its "expected" value. In this approach, by properly amplifying the difference signal, ADC full scale amplitude can be used to convert a voltage whose values cover only few DAC LSB. In other words, the ADC full scale is used to analyze only the DAC error span, thus providing the needed resolution. Moreover, particular attention must be paid to choose properly the CMRR of the differential amplifier because to its inputs are connected signals with high common mode voltages.

A similar solution, for dynamic characterization, based on the use of a low-resolution ADC to digitize the difference between the DAC output and a reference voltage, is given in [9]; the corresponding measurement station is sketched in Fig.2. A reference waveform generator is adopted to provide a sinusoidal signal whose amplitude and phase are,

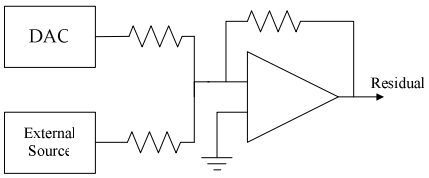

Fig. 2. Scheme of the proposal in [9] for dynamic characterization of DACs.

respectively, equal and opposite to those generated by the DAC. The signals are connected to the input of an adder circuit whose output is the residual voltage that has to be digitized through the ADC.

For both the previous solutions, some practical issues have necessarily to be taken into account for the hardware implementation of the method. A critical point is the use of an auxiliary source as reference voltage, common to other solutions already presented in literature [10-11]. Differently from the static characterization, when the output voltage of the DAC is variable versus time, it is, in fact, necessary to suitably synchronize the source with the DAC under test. To this aim, a phase-locked circuit has to be adopted that could introduce distortions on the reference signal provided by the external source. In these paper, moreover, no analysis of the effects of either amplitude or phase differences between DAC output and reference signal on the acquired amplified voltage and, consequently, on the estimates of the DAC errors.

3. THE PROPOSED METHOD

In Fig.3, a block diagram of the proposed method is shown; the basic idea underlying the method consists in acquiring and digitizing the difference between the output voltage generated by the DAC and a reference signal. Reference signal cannot be generated by an external, auxiliary source, due to the difficulty to grant a reference voltage that would have the same frequency and phase of the output provided by the DAC. To this aim, the authors have stated that the reference signal have to be extracted from the signal generated by the DAC itself.

With specific regard to the signal to be adopted in the test, it has to be a sinusoidal waveform; such a signal presents, in fact, two main advantages: *(i)* the signal is characterized by an evolution versus time completely defined in analytical way, and *(ii)* reference waveform characterized by high level of spectral purity can be generated thanks to a proper filter bank.

As stated above, the basic idea consists of digitizing through the ADC the amplified difference between the sinusoidal output voltage of the DAC and the reference sinusoidal signal, also referred in the following as v_{ampl} signal; two possible solutions, respectively shown in Fig.4 and Fig.5, can be adopted to the purpose.

With regard to the first solution (Fig.4), the signal generated by the DAC passes through the cascade of a notch filter and an amplifier characterized by a gain equal to G_d; as for the second solution, it exploits a bandpass filter and a differential amplifier that provides the difference between the DAC and filter output signal. From a theoretical point of view, both solutions are equivalent, but they highly differ if practical implementation issues are considered.

Both notch and bandpass filter modify their input signal. To this aim, three features would desirable in filter design: high roll-off, linear phase shift and constant gain response versus frequency. Unfortunately, it is not possible to achieve all the features simultaneously.

If a notch filter is adopted, a non-linear phase shift and variable attenuation of the different frequency components has to be expected according to the specific characteristics of the implemented filter [12]. The error signal of the DAC acquired by the ADC is, thus, affected by the distortion introduced by the filter. On the contrary, if the solution

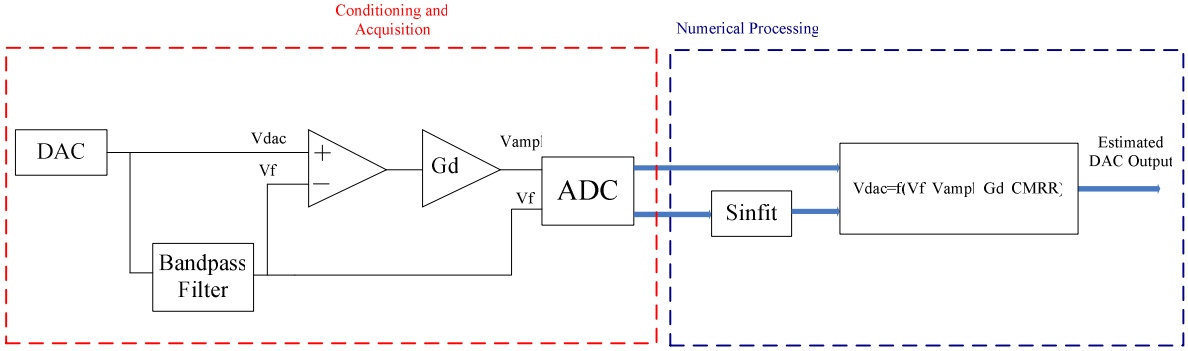

Fig. 3. Block diagram of the proposed test method.

based on bandpass filter and instrumentation amplifier is adopted, the output of the filter mainly consists of a single component, the frequency of which is equal to the fundamental frequency of the DAC output signal. This component may be characterized by phase shift and attenuation with respect to the filter input signal, but those

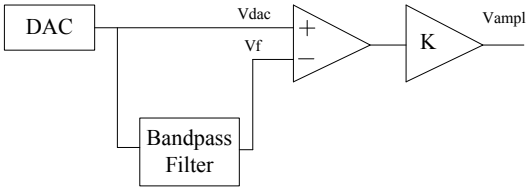

Fig. 4. Conditioning scheme with bandpass filter.

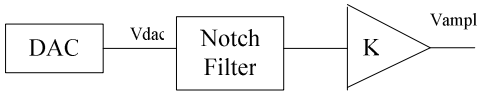

Fig. 5. Conditioning scheme with notch filter.

parameters can be estimated because the output signal *(i)* is undistorted and *(ii)* it is a waveform that can be analytically expressed (a sinewave), therefore a numerical fit can be applied.

In conclusion, the method of Fig.5 requires a high performance filter, which should exhibit linear phase and flat gain among a wide range frequency. Method performance being equal, thus, the operating configuration shown in Fig.4 proves to be less expensive and it has been adopted for the implementation of the measurement station.

The output voltages of the DAC, v_{DAC}, and filter, v_f, are connected to the inputs of the differential amplifier, that provides the output voltage v_{ampl} given by:

$$v_{ampl} = G_d\left(v_{DAC} - v_f\right) + G_c\left(\frac{v_{DAC} + v_f}{2}\right) \qquad (1)$$

where G_d is the amplifier differential gain and G_c is the common mode gain, attainable from the amplifier CMRR. Equation (1) suggests that if G_d and G_c are known and if v_{ampl} and v_f are acquired, the DAC output can be estimated. A two-channel ADC, thus, is employed with the aim of sampling and converting the filter and amplifier outputs. Obviously, v_{DAC} and v_f have to be digitized with a resolution lower than the DAC LSB. At this aim,. The filter output, acquired according to the ADC number of bits, is interpolated by means of a sine-fit algorithm [13], in order to reconstruct v_f with a much higher resolution. As regards v_{ampl}, this signal is an amplified version of the DAC error that can be digitized by an ADC with a resolution lower than that of the DAC under test.

Once the v_{ampl} signal has been acquired, the corresponding samples have to be processed in order to remove some artifacts introduced by the conditioning block. In particular, the following problems have to be faced:

1. different amplitude between the signal generated by the DAC and the filter output
2. phase shift between the signal generated by the DAC and the filter output
3. finite value of the CMRR of the differential amplifier, whose input signals exhibit high common mode voltages.

Their effect on the amplified voltage v_{ampl} is the presence of a sinusoidal component superimposed to the error acquired by the ADC, that does not contain information about the DAC errors. The sinusoidal component due to gain and/or phase error of the filter does not affect the reconstruction process of DAC output, that is based on equation (1) applied on the instantaneous values. The contribution due to the amplifier finite CMRR, instead, cannot be recognized and removed; hence the employed amplifier and operating conditions should assure a CMRR as higher as possible.

It is worth noting that the digital processing allows to reconstruct the DAC output, regardless of the artifacts affecting the amplifier output, but it is, however, necessary to implement the measurement station in such a way to reduce their impact. The presence of a high sinusoidal voltage affecting the output signal of the amplifier could, in fact, saturate the ADC; it would be so needed to reduce the gain of the amplifier, thus causing a degradation of measurement resolution.

4. HARDWARE IMPLEMENTATION

The achievable resolution for the DAC characterization depends on different factors associated with the DAC number of bits, the CMRR of the differential amplifier, the range and the number of bits of the exploited ADC. In [14] the analytical relationship among the desired resolution and these parameters has been deeply investigated and the specifications required to the devices employed in the measurement station have been determined. This theoretical study allowed to define the measurement station realized for the preliminary tests, shown in Fig. 6.

The DAC under test is a waveform generator Agilent 33220A, which makes use of a 14 bits converter and has a range tunable from 100mVpp up to 20Vpp.

The bandpass filter is a Wavetek 716, whose main characteristics are:

- 1 Hz to 100 kHz Frequency Range
- 115 dB/Octave Rolloff
- Passband Ripple: 0.8 dB
- Stopband Attenuation: 80 dB min
- The mainframe contains a 7^{th} order elliptic low-pass filter and a 7^{th} order elliptic high-pass filter, that can be connected in cascade for obtaining a narrow-bandwidth band-pass filter. In order to reduce the pass-band attenuation of the band-pass filter, the cut-off frequency of the low-pass filter is slightly higher than the nominal one and the cut-off frequency of the high-pass filter is slightly lower than the nominal one.

The differential amplifier is realized with an instrumentation amplifier ADA400A by Tektronix, whose characteristics are:

- Programmable gain from 0.1 to 100
- For a differential gain equal to 100, the *CMRR* evolution, versus frequency, is shown in Fig. 6: it reaches 100dB within the range 10-10000 Hz, but it get worse as the frequency of the generated signal increases.

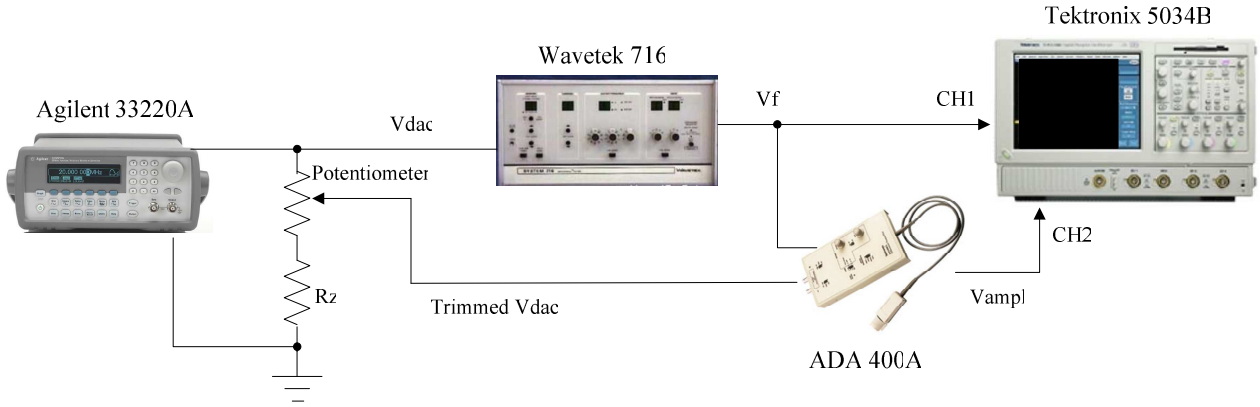

Fig. 6. Scheme of the implemented hardware test station.

As stated above, gain and phase errors due to the filter cause a sinusoidal component, affecting the amplifier output, that determines the increase of ADC range and, consequently, a lack of resolution. In order to minimize the sinusoidal component, these solution have been performed:

- a tunable attenuator between DAC and differential amplifier, capable of granting that a signal amplitude as close as possible to the filter output; in particular, a high precision potentiometer with a linearity of 0.25% has been employed.
- the frequency of the DAC output signal has to be tuned in such a way that its frequency does not undergo phase shift through the band-pass filter.

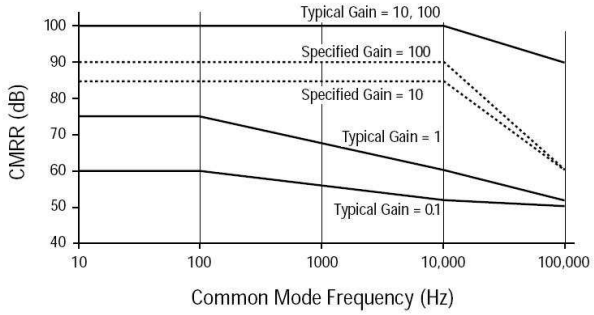

Fig. 7. CMRR evolution of ADA400A versus frequency.

The potentiometer resistance and the signal frequency are tuned according to a proper algorithm aiming at minimizing the root mean square of the amplifier output voltage.

As the reference ADC has been used the Tektronix digital scope, model TDS5034B, whose main characteristics are summarized as follows:

- 8 bits resolution ADC
- 4 vertical channels with voltage ranges tunable from 1mV/div up to 10V/div
- Acquisition memory depth of 2 MS
- Maximum sampling frequency up to 5GS/s

Only two channels are exploited in this setup. The first one acquires the bandpass filter output; the samples, that have been quantized according to the ADC resolution are, successively interpolated by means of a sine-fit algorithm, in such a way that the analytical formula of the reference signal is obtained. The second channel, instead, has to acquire the voltage v_{ampl} at the output of the differential amplifier. The gathered samples are, then, combined according to expression (1) in order to gain an estimate of DAC output.

5. EXPERIMENTAL RESULTS

In this section the preliminary results obtained in experimental tests conducted through the measurement station described in the previous section are presented. All tests have been executed by means of a sinusoidal signal, whose amplitude has been set equal to 8 V_{pp}.

In the generator memory it has been stored a codes sequence of 65536 samples representing the digital version of one period of a sinusoidal waveform. In order to stimulate all the DAC codes, in fact, the length N_{DAC} of the codes sequence has to satisfy the inequality:

$$N_{DAC} \geq \pi \cdot 2^{14} = 51472 \qquad (2)$$

Moreover, for reducing the number of acquisition needed the test signal frequency has been selected in such a way that, in each period, all the DAC codes are tested. Since the DAC employs a Direct Digital Synthesis algorithm for varying with high resolution the frequency of the generated waveform, the stimulus of all the codes is assured if it is satisfied the relationship:

$$\frac{N_{DAC} \cdot f}{f_g} \leq 1 \qquad (3)$$

where f is the signal frequency and f_g is the generation rate. Agilent 33220A exhibits a generation frequency of 50MHz; since N_{DAC} is equal to 65536, equation (3) provides the maximum signal frequency, which is: 762.9 Hz.

Consequently, the test signal frequency has been chosen equal to 100Hz.

The full scale amplitude of the two input channels of the DSO, referred to as CH1 and CH2, have been set to 10 V and 20 mV. The sampling frequency is 5MS/s and 100kS per channel have been recorded. Fig.8 shows the signal

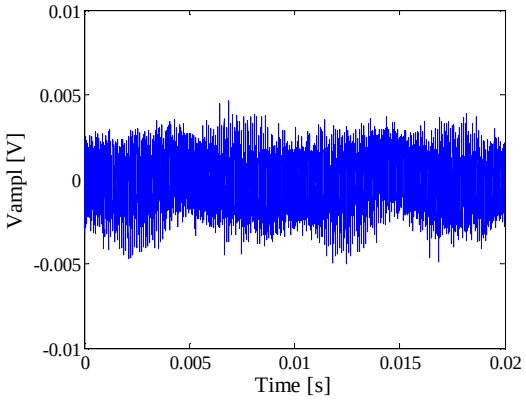

Fig. 9. v_{ampl} signal after amplitude and frequency correction.

acquired on CH2, accounting for the voltage v_{ampl} provided by the differential amplifier before the adjustment of amplitude with potentiometer and frequency and, thus, affected by a severe sinusoidal component. On the contrary, in Fig.9 the same signal is plotted after the correction of amplitude and frequency. The cancellation of the sinusoidal component due to filter attenuation and phase displacement allows to switch the CH2 range from 20mV to 10mV, thus gaining an improvement by two in terms of resolution.

The obtained signal is, obviously, still characterized by the noise introduced by the differential amplifier. The noise introduced by the differential amplifier has been limited by averaging the samples obtained from repeated acquisitions. Fig.10, as an example, shows the amplifier output after the

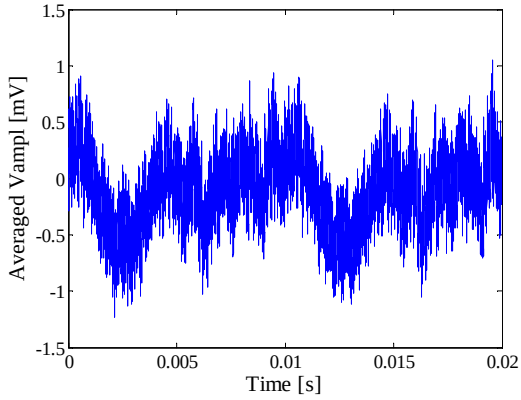

Fig. 10. Averaged v_{ampl} signal.

averaging on 30 acquisitions.

The final step is the combination, according to equation (1) of the signal obtained as the sum of *(i)* the sinusoidal voltage acquired on CH1 and interpolated through a standard three parameters sin-fit, and *(ii)* the noise signal gained as in previous step; it can, practically, been considered as the "true" voltage signal generated by the DAC.

6. CONCLUDING REMARKS

In the paper a method for the dynamic characterization of high resolution digital-to-analog converters has been proposed. It is based on the employment of a low resolution ADC for the acquisition of the error signal obtained by the difference between the voltage generated by the DAC and a reference signal. Choosing the test signal as a sinusoidal waveform, the reference signal has been attained by means of a narrow passband filter. A differential amplifier, then, expands the difference between the DAC output and the reference signal.

The paper is mainly focused on the issues related to the hardware implementation of the measurement station. It has been performed, in fact, a complete survey of the observed non idealities of the employed devices, their impact on the measurement accuracy and the solutions adopted in order to maintain the needed resolution.

The experimental results gained through the described measurement station proves that the DAC output has been retrieved with a very high resolution. The error signal, in fact, has been digitized by means of an ADC with a number of bits equal to 8, whose range has been set to 10mV, achieving a resolution equal to 39.2µV. The LSB used by the DAC, which has the use of 14 bits and is generating a signal whose amplitude is equal to 8Vpp, is equal to 488µV. The DAC output, hence has been gained with a resolution twelve times lower than DAC LSB. The measurement method, thus, is equivalent to a scheme where the DAC voltage is acquired by means of an ADC with a range of 8V and a number of bits equal to:

$$N_{eq} = \log_2\left(\frac{8V}{39.2\mu V}\right) = 17.6$$

The presented measurement method allows gaining the time evolution of the DAC output voltage. For obtaining the DAC characteristic it is necessary to know the DAC codes associated to the acquired voltage samples. At this aim, the ongoing activity is focused on the identification of a proper timing association procedure able to correlate the DAC voltages to the codes at DAC input.

REFERENCES

[1] P.P. Fasang, "Optimal selection of test vectors for DA

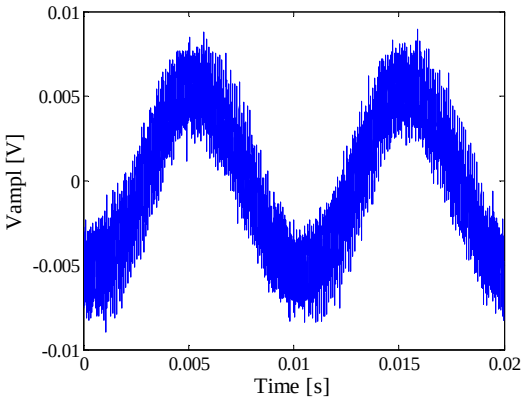

Fig. 8. Acquired v_{ampl} signal.

converter testing", *Measurement*, Vol. 31, N. 3, pp. 165-174, 2002.

[2] D. Grimaldi, D.L. Carni, **"**Static Characterization of High Resolution DAC Based on Over Sampling and Low Resolution ADC", *Proc. of IEEE Instr. And Meas. Tech. Conf. IMTC*, pp. 1–6, 2007.

[3] Balestrieri, E., Daponte, P., Rapuano, S., "Digital to analog converter: a metrological overview", *Proc. of 9th Workshop on ADC Modeling and Testing*, 2004.

[4] "Draft Standard for Terminology and Test Methods for Digital-to-Analog Converters", IEEE std P1658, September 2008.

[5] L. Angrisani, M. D'Apuzzo, M. D'Arco, "Fast transformation for DAC parameter identification," *IEEE Transactions on Instrumentation and Measurement*, vol.55, No.6, December 2006, pp.2007-2013.

[6] Le Jin, Hosam Haggag, R. Geiger, Degang Chen, "Testing of Precision DACs Using Low-Resolution ADCs with Dithering", *IEEE International Test Conference*, pp.1–10, 2006.

[7] Le Jin, Hosam Haggag, R. Geiger, Degang Chen, "Testing of Precision DACs Using Low-Resolution ADCs with Wobbling", *IEEE Transaction on Instrumentation and Measurements*, Vol. 57, N. 5, pp. 940-946, 2008.

[8] S. Max, "Optimum DAC and ADC Testing", *Proc. of IEEE Intern. Instr. And Meas. Tech. Conf. I^2MTC*, pp. 573–578, 2008.

[9] Fang Xu, "Signal Cancellation Technique for Testing High-end Digital-to-Analog Converters", *Proc. of IEEE Instr. And Meas. Tech. Conf. IMTC*, pp. 1-4, 2007.

[10] K. Arabi, B. Kaminska, M. Sawan, "On chip testing data converters using static parameters", *IEEE Trans. On Very Large Scale Integr. Systems*, Vol. 6, N. 3, pp. 409-419, 1998.

[11] Chun Wei Lin, Sheng Feng Lin, Shih Fen Luo, "A new approach for nonlinearity test of high speed DAC", *IEEE Int. Workshop on Mixed-Signals, Sensors, and Systems*, pp. 1-5, 2008.

[12] Kendall L. Su, Analog Filters, Springer, 2002.

[13] IEEE Std 1241-2000: Standard for Terminology and Test Methods for Analog-to-Digital Converters, 2000.

[14] M. D'Arco, A. Liccardo, M. Vadursi, "Design of a test equipment for DAC's performance assessment", Accepted for publication in *Proc. of IEEE Intern. Instr. And Meas. Tech. Conf. I^2MTC*, 2009.