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PORTABLE ANALYZER FOR IMPEDANCE SPECTROSCOPY

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Abstract – The paper presents an impedance analyzer designed for impedance spectroscopy of objects located in the field. The use of the specialized microsystem AD5933 was assumed. The analysis and tests of the microsystem in the configuration proposed by the manufacturer showed the limitations having meaningful influence on the impedance measurement accuracy. In order to eliminate disadvantages of the microsystem, a new solution using two AD5933 microsystems was proposed. This solution allows to measure impedance in a wide range of $100\ \Omega \leq |Z_x| \leq 10\ G\Omega$ at measurement frequencies in the range of 0,01 Hz ÷ 100 kHz.

Keywords: impedance spectroscopy, impedance analyzer,

1. INTRODUCTION

Impedance spectroscopy is a method widely used for testing of biological and physicochemical objects. It is used in e.g.: biomedical measurements [1], corrosion monitoring and diagnostics [2], materials research [3], batteries and fuel cell performance controlling [4]. Many times the tests are performed on objects located directly in the field. An example of such use of impedance spectroscopy is the testing of the performance of anticorrosion coatings on objects directly in the field e.g. on bridges, pipelines and other steel structures. This implies the need of development of portable instrumentation for impedance spectroscopy of objects located in the field.

There are no commercially available impedance analyzers, miniaturized enough, which would enable wireless communication between the measuring device, installed in a difficult-to-reach place, and a personal computer controlling the analyzer. Due to these facts, developments have been performed on realization of a portable analyzer which resulted in the prototype presented in [5] and also the construction developed by the authors which will be presented here.

The realized portable analyzer for impedance spectroscopy is based on the System-on-Chip microsystem (SoC) AD5933 by Analog Devices. The advantages of the AD5933 chip are low power consumption and integration of most blocks required for impedance spectroscopy. The chip contains the following blocks: a sinusoidal signal generator, AD converter, hardware DFT module. The analysis and test of the chip in the configuration suggested by the manufacturer and performed by the authors showed limitations of the chip in the impedance analyzer. The most important ones are: a too narrow range of the measured impedance modulus 1 kΩ ÷ 10 MΩ and measurement frequencies 1 kHz ÷ 100 kHz, the need of additional measurement for calibration, the lack of constant output resistance and possibility of spectrum leakage while determining DFT. Because of this, the paper presents the analyzer solution based on two AD5933 chips and extended input circuitry, which allows to reduce the influence of the chip's disadvantages on the accuracy of the impedance measurement.

2. PROPOSED IMPEDANCE ANALYZER

The need of development of a portable, miniaturised impedance analyzer moved the authors to use two AD5933 chips to construct the impedance analyzer (Fig. 1). It is proposed to use the SoCs in a new configuration, different than that suggested by the manufacturer in his application note [6]. In the following parts of the paper, the reasons arguing for the benefits of the used solution will be presented and show the limitation of the basic configuration of the AD5933 proposed by the manufacturer.

The SoC contains analog blocks as well as digital ones necessary to realize the impedance measurement using a method based on the DSP technique. The SoC is equipped with an I^2C interface used for controlling and reading the internal registers of the microsystem (unfortunately the I^2C address of the SoC is fixed by the manufacturer and excludes the use of more than one chip on the same I^2C bus). In the SoC, one can distinguish two paths: the excitation signal generation and the determination of orthogonal parts of the measurement signal. The sinusoidal signal generation is performed using the method of direct digital synthesis (DDS). This path consists of a 27-bit DDS core, a D/A converter and amplifier A1 with programmable gain and output resistance R_{out}. In the measurement signal path, the signal from the amplifier A2 is applied to a low-pass (antyaliasing) filter and then sampled and quantized by a 12-bit A/D converter. The calculation of the real and imaginary parts of the signal on the basis of the acquired samples is performed in the module of discrete Fourier transformation (DFT).

The main disadvantage of the configuration proposed by the manufacturer is the use of only one AD5933 chip, allowing the measurement of orthogonal parts of only

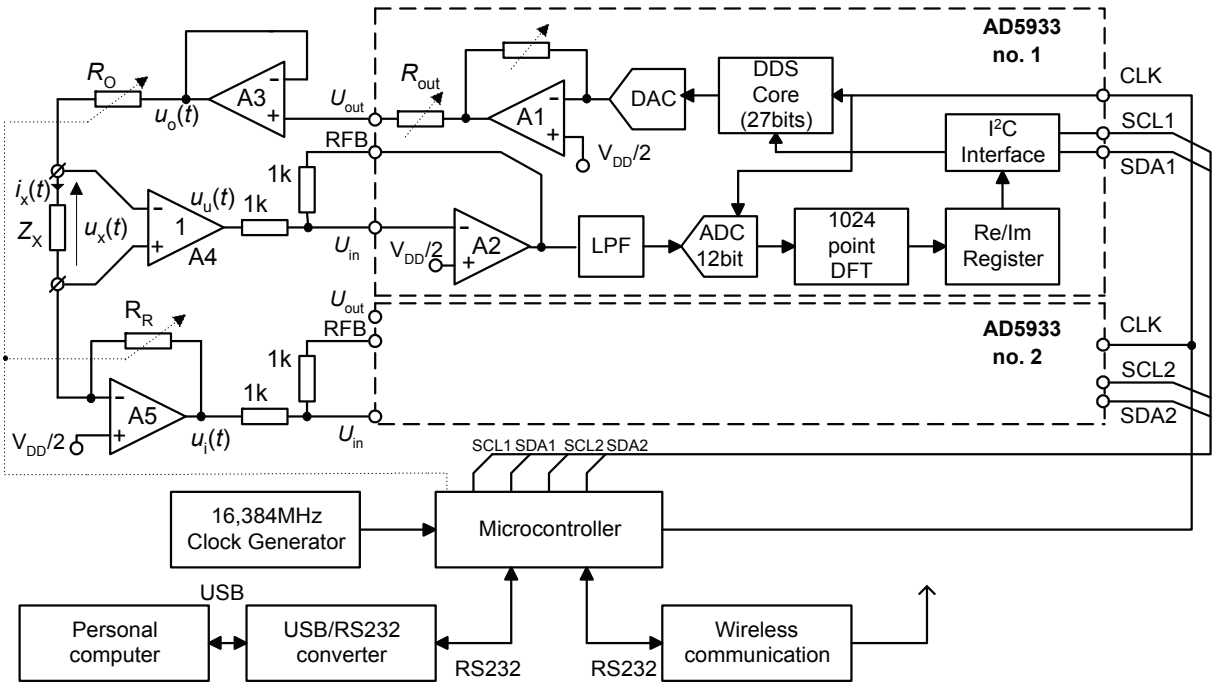

Fig. 1. Block diagram of the impedance analyzer.

current flowing through the measured impedance. Because to calculate the impedance, it is necessary to know the voltage across the measured impedance, so the manufacturer assumes two measurement cycles: calibration and normal. During calibration, the measured impedance is replaced by the reference resistor R_{cal}, which allows to determine the voltage across the measured impedance. The two-stage algorithm proposed by the manufacturer is onerous to realize, but also leads to very large errors (see subsection 2.1). Due to this fact, the authors used simultaneous measurement of voltage and current (eliminating the calibration stage) using two AD5933 chips. The block diagram of the developed analyzer is presented in Fig. 1.

The first SoC is used to generate the excitation signal and to determine Re and Im parts of signal $u_u(t)$ proportional to the voltage $u_x(t)$ across the measured impedance Z_x. The second SoC realizes the measurement of orthogonal parts of signal $u_i(t)$ proportional to current $i_x(t)$ flowing through Z_x.

The extraction of signals u_u and u_i is realized by the input circuitry (amplifiers A3 ÷ A5) connected to the SoC chips. To measure the voltage, the differential amplifier (A4) with gain equal to 1 was used, but the current measurement is performed with the aid of current-to-voltage converter (A5). Amplifiers A2 in both AD5933 chips work with negative unity gain (-1) obtained by connecting external 1 kΩ resistors. In the realized analyzer, the measured impedance is calculated according to the definition, on the basis of (1):

$$|Z_x| = \sqrt{\frac{(\mathrm{Re}U_u)^2 + (\mathrm{Im}U_u)^2}{(\mathrm{Re}U_i)^2 + (\mathrm{Im}U_i)^2}}\, R_R,$$

$$\varphi_{Z_x} = arctg\frac{\mathrm{Im}U_u}{\mathrm{Re}U_u} - arctg\frac{\mathrm{Im}U_i}{\mathrm{Re}U_i}, \qquad (1)$$

where: R_R – range resistor of the current-to-voltage converter (A_5),
$\mathrm{Re}U_u$ and $\mathrm{Im}U_u$, $\mathrm{Re}U_i$ and $\mathrm{Im}U_i$ – orthogonal parts of signals u_u and u_i, read from SoC registers.

Because I^2C addresses of both SoCs are identical, the microcontroller communicates with AD5933 chips using separate buses. To correctly calculate the impedance from (1), it is necessary to determine orthogonal parts of signals $u_u(t)$ and $u_i(t)$ in relation to the same coordinates. Assuring this condition is possible when excitation signals (U_{out}) in both chips are generated synchronously (exactly in the same phase). The synchronization is obtained by using a common clock signal (CLK) and simultaneous initiation of the measurement in both SoCs, realized by microcontroller and I^2C interfaces.

2.1. Elimination of the influence of output resistance and extension of the measurement range of the impedance modulus

The measurement algorithm given by the manufacturer (using only one AD5933 chip) assumes that the amplitude of the output voltage U_{out} (at the fixed measurement frequency f_m) is constant. The value of this voltage is determined during the calibration phase on the basis of the measurement of the current flowing through the reference resistor R_{cal}. Performed tests of the SoC chip showed that the condition U_{out} = const is not fulfilled, because resistance R_{out} is not constant and creates a voltage divider with the measured impedance Z_x. When calculating the measured impedance value according to the formula given by the manufacturer [6]:

$$Z_x = \frac{1}{GF\left(\mathrm{Re}\,X_{meas} + j\,\mathrm{Im}\,X_{meas}\right)} \qquad (2)$$

where: $GF = \dfrac{1}{R_{cal}\left(\mathrm{Re}\, X_{cal} + j\, \mathrm{Im}\, X_{cal}\right)}$ – Gain Factor determined during the calibration stage,

$\mathrm{Re}X_{cal}$ and $\mathrm{Im}X_{cal}$, $\mathrm{Re}X_{meas}$ and $\mathrm{Im}X_{meas}$ – orthogonal parts read from SoC registers sequentially in the calibration stage and measurement stage,

the measured impedance modulus is different than the reference resistor used for calibration, the obtained error is greater (Fig. 2).

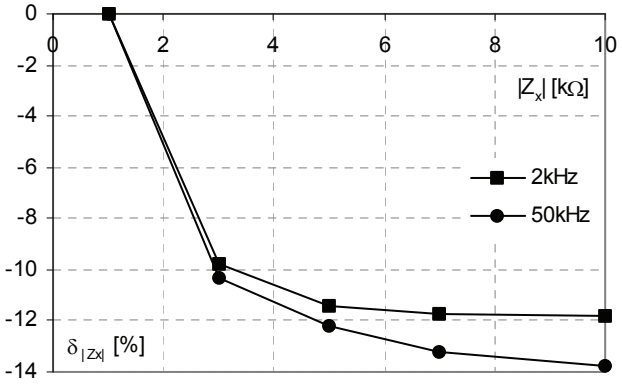

Fig. 2. Error of the impedance modulus measurement in AD5933 chip, in the configuration suggested by the manufacturer, for nominal R_{out} = 200 Ω, R_{cal} = 1 kΩ and f_m = 2 kHz and 50 kHz.

The inacceptable measurement error and the need of performing calibration for each measurement frequency mainly caused the rejection of the manufacturer's configuration with a single AD5933 chip. The use of simultaneous measurement of voltage and current with the aid of two SoCs does not require the assuring condition of constant amplitude of the output signal ($U_{out} \neq$ const).

In order to extend the measurement range of the analyzer towards high impedances up to $|Z_x| \leq 10$ GΩ, the amplifiers in the input circuitry must be characterized by low input currents (of the level of a few pA) and high differential and common input impedance (Z_{dif}, Z_{cm}) while assuring a bandwidth as wide as possible. Because input amplifiers of the AD5933 chip do not meet these requirements, the analyser was equipped with additional input circuitry (A3 ÷ A5). The AD8646 amplifiers were used, which are characterized by an input current not exceeding 1 pA (at 25°C), the impedances Z_{dif} and Z_{cm} are determined by resistances $R_{dif} = R_{cm}$ = 10 TΩ and capacitances C_{dif} = 2,5 pF and C_{cm} = 7,8 pF and they have a wide bandwidth GBW = 24 MHz.

To assure a wide range of the impedance measurement (it is required to change the current i_x range from 10 pA to 1 mA in the current-to-voltage converter A5), range resistors R_R (100 Ω,...100 MΩ, 1GΩ) switched in decade with the aid of miniature reed-relays have been used. The value o resistance R_R is selected in relation to $|Z_x|$ to keep gain K of amplifier A5 in range $-0{,}01 < K \leq -0{,}1$. Simultaneously with the change of measurement range, the resistance R_o at the output of voltage follower A3 is changed. The voltage follower applies the measurement signal to the measured impedance Z_x. Resistor R_o ($R_o = 0{,}1\ R_R$) limits the current flowing into the input of the current-to-voltage converter in case of Z_x shortage and prevents the differentiation of slopes of the stair-shaped signal approximating a sinusoidal signal.

2.2. Reduction of spectrum leakage and extension of the measurement frequencies range

All digital blocks and the DAC and ADC of the AD5933 chip are clocked from a common source of the clock signal with frequency f_{clk}. In order to obtain information how f_{clk} influences the frequency of the measurement signal f_m and sampling frequency f_s, clock distribution in SoC was analyzed (Fig. 3). This allows to estimate for which measurement frequencies the spectrum leakage in DFT calculation does not appear. It is well-known that for harmonic signals, the spectrum leakage does not appear, when samples of signal are acquired in the integer number L of periods of signal, what can be described by (3):

$$L f_s = N f_m \tag{3}$$

where: N = 1024 – number of samples acquired in AD5933.

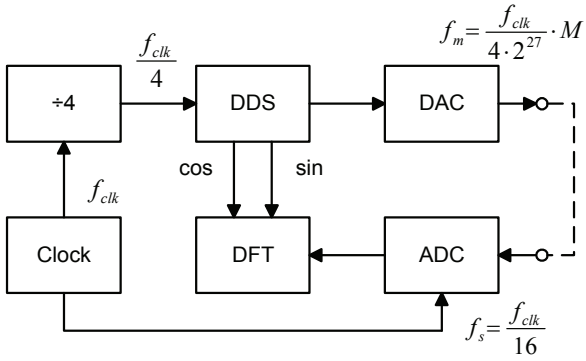

Fig. 3. Clock distribution in AD5933.

Taking into account the formula describing the frequency f_m of the measurement signal generated in AD5933 using the DDS method [6] (Fig. 3) and (3) we obtain: $L = M/2^{15}$. As we can see, the clock frequency has no influence on spectrum leakage, only the value of M programming the measurement frequency is important. The tests of influence of spectrum leakage on the error of impedance measurement have been performed by changing the measurement frequency (by programming M) that is changing the number of acquired periods (Fig. 4). It can be seen that for an integer number of periods (e. g. L = 4), the error is the lowest, but when L is exactly in the middle between two integer values (e. g. L = 3,5) the error caused by the leakage is the greatest. It can be also noticed that the influence of the samples acquired in the part of period on the measurement error is getting lower when the number of the acquired periods increases.

The AD5933 chip allows to measure an impedance spectrum in the range 1 kHz ÷ 100 kHz using the internal clock [6]. A much wider measurement frequency range is required in case of impedance analyzers. The construction of the AD5933 chip makes the use of an external clock source possible, allowing to scale flexibly the clock, thus allowing to generate signals at frequencies below 1 kHz.

While designing the range of measurement frequencies, it is necessary to choose such clock frequencies f_{clk} which allow to obtain a frequency grid in range of 0,01 Hz÷ 100 kHz (10 frequencies with equal step Δf_m in each decade) for which there is no spectrum leakage. When choosing f_{clk} it is also important to take into account the time of acquisition of 1024 samples (T_{meas}) of measurement signals u_u and u_i, in order to perform the DFT operation. If $T_{meas} = 20$ ms or when it is a multiplication of the period of the noise signal caused by power supply lines (50 Hz), the influence of noise will be eliminated in the DFT calculation. This condition is important in case of measurement of high impedances ($|Z_x| > 10$ MΩ), at frequencies $f_m < 1$ kHz.

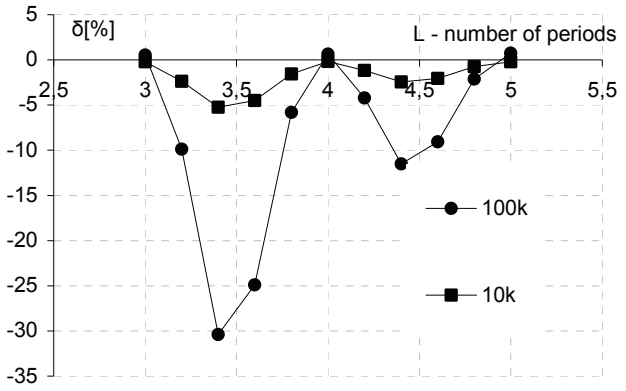

Fig. 4. Relative error of the impedance modulus measurement (at the beginning of the range $|Z_x| = 10$ kΩ and at the end of the range $|Z_x| = 100$ kΩ).

Taking into account the relation between f_{clk}, f_m and f_s (Fig. 3), an external clock source (16,384 MHz) was used (Fig. 1) which has six programmable values of f_{clk} assuring the above conditions. Table 1 presents parameters of the generated signal, number of periods (L) and acquisition time (T_{meas}), when samples are collected by the ADC.

Table 1. Measurement signal parameters.

f_{clk} [Hz]	f_m [Hz]	Δf_m [Hz]	L	T_{meas} [s]
8,192 M	10 k-100 k	10 k	20-200	2 m
819,2 k	1 k-9 k	1 k	20-180	20 m
	100-900	100	2-18	
81,92k	10-90	10	2-18	0,2
8,192 k	1-9	1	2-18	2
819,2	0,1-0,9	0,1	2-18	20
81,92	0,01-0,09	0,01	2-18	200

The THD coefficient of the generated signal was also taken into account when designing the frequency ranges. The harmonic signal is generated using approximation by a staircase waveform. The quality of measurement signal shape decreases when L increases, because the output signal contains a lower number of samples in each period. In the realized analyzer, the number of samples in the period of generated signal ($1/f_m$) changes from 2048 (for lower frequency) down to ca. 22 for the highest frequency in each subrange of frequency, assuring a THD coefficient at a level better than a few percent even in the worst case.

3. EVALUATION OF THE REALIZED PROTOTYPE OF THE IMPEDANCE ANALYZER

The prototype of the impedance analyzer was realized in the form of a virtual instrument. A PC connected via USB to the measurement module is used to control the analyzer (Fig. 1). The graphical user interface (GIU) (Fig. 5) was

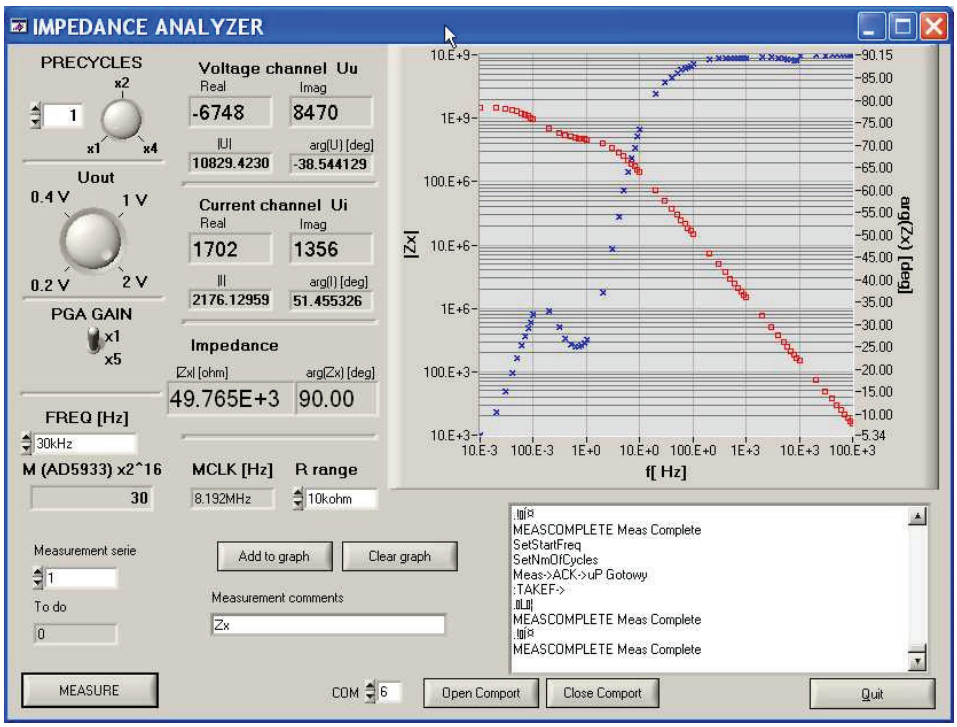

Fig. 5. Graphical user interface for controlling impedance analyzer.

designed to allow programming of the measurement parameters (amplitude and frequency of the measurement signal) and visualization of the measured value of the modulus and argument of the tested object (calculated by the PC on the basis of (1)). In order to present the results of impedance spectroscopy of the tested object in the form of a Bode plot of modulus and argument of impedance as a function of frequency, a separate window was assumed.

Each impedance measurement cycle for a specified frequency can be preceded by additional periods of the measurement signal (precycles). This is an important function in case of the measurement of the object with a long time constant in relation to the measurement signal period, because it allows to stabilize the measurement condition caused by a transitional state. There is the possibility, offered by the GUI, to perform the measurement series, allowing to average the results in case of noise, especially when measuring high impedances $|Z_x| > 1$ GΩ.

The developed GUI is used to debug and test the realized prototype, so the additional windows present helpful information including the real and imaginary parts of the signals proportional to voltage (U_U) across and current (U_I) through the measured impedance (presented as decimal numbers determined on the basis of bipolar binary codes read from registers of AD5933 microsystems) and messages sent via USB between the PC and the measurement module.

In order to determine the accuracy of the impedance measurement, tests of the analyzer were performed. As the test object, the reference two-terminal RC network presented on Fig. 6 was chosen. The configuration and component values of the two-terminal network correspond to the typical example of the equivalent circuit of the anticorrosion coating in the early stage of exploitation.

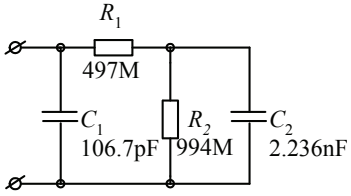

Fig. 6. Schematic diagram of the reference two-terminal RC network.

The selected RC network is a representative example of impedance spectroscopy use to monitor the performance of the anticorrosion coatings on the objects directly in the field. The developed portable and miniaturized analyzer is designed to work with such kind of objects. The capacitors in the two-terminal network were measured using a precise impedance meter E4980A with an error not exceeding 0,1%, and resistors were measured using the technical method with the aid of a reference resistor 10 MΩ±0,01% and a 34401A multimeter.

The series of 10 measurements of the two-terminal network has been performed at frequencies in the range of 100 kHz – 0,01 Hz (with 1-2-5 steps), using signals with an amplitude of 1V_{RMS}. The mean values of the obtained results of modulus and argument of the impedance are presented in Fig. 7. For each measurement point the standard deviation of the impedance modulus does not exceed 0,4%, and for argument it is lower than 0,2° in the whole measurement frequency range. The graph also presents the curves for modulus and argument of impedance of the tested two-terminal network calculated theoretically on the basis of RC component values.

The graphs of impedance characteristic of the two-terminal RC network (presented in Fig. 7), due to the wide range of changes of impedance modulus (10 kΩ ÷ 1.5 GΩ) and argument (90° ÷ 5°), do not allow to precisely evaluate the measurement accuracy. So, taking values calculated theoretically as real, the relative errors of modulus and absolute errors of argument of impedance have been determined (Fig. 8).

When analyzing graphs, the cyclic increase and decrease of the measurement errors of impedance modulus and argument can be noticed. It is caused by the change of the frequency of the measurement signal generated with the aid of approximation via stair-shape wave (DDS method). Using such a signal to measure the impedance Z_x (of two-terminal RC network) in the circuit presented in Fig. 1, the slopes of the excitation signal are differentiated (amplifier A5 with R_R resistor in a feed-back loop and Z_x impedance in the input create differentiating configuration). So, the sinusoidal signal $u_i(t)$ is distorted by impulses in points where slopes of the stair-wave exist in the excitation signal.

According to the rule presented in Table 1, the approximation of the signal is realized with the variable number of stair-steps for each frequency in decade. Thus, the number of pulses noising signal $u_i(t)$ changes in the same

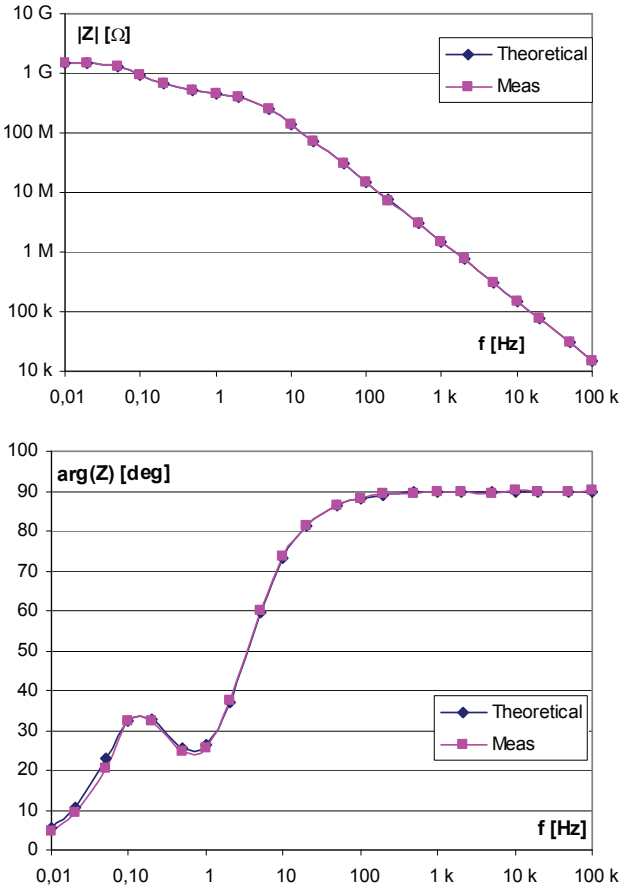

Fig. 7. Impedance modulus and argument of the tested object.

way in each decade and similarly influences the impedance measurement error. In order to lower the noising impulses, R_o resistor changes simultaneously with R_R were used. This resistor allows to decrease the effectiveness of the existing differentiating circuit. The performed tests showed that the used solution is not effective enough and in the final version of the analyzer it is necessary to use an additional low-pass filter with band-pass frequency switched in decadely at the output of A3 amplifier. The filter should smooth the generated measurement signal enough to make the differentiation of slopes of the stair-wave unimportant.

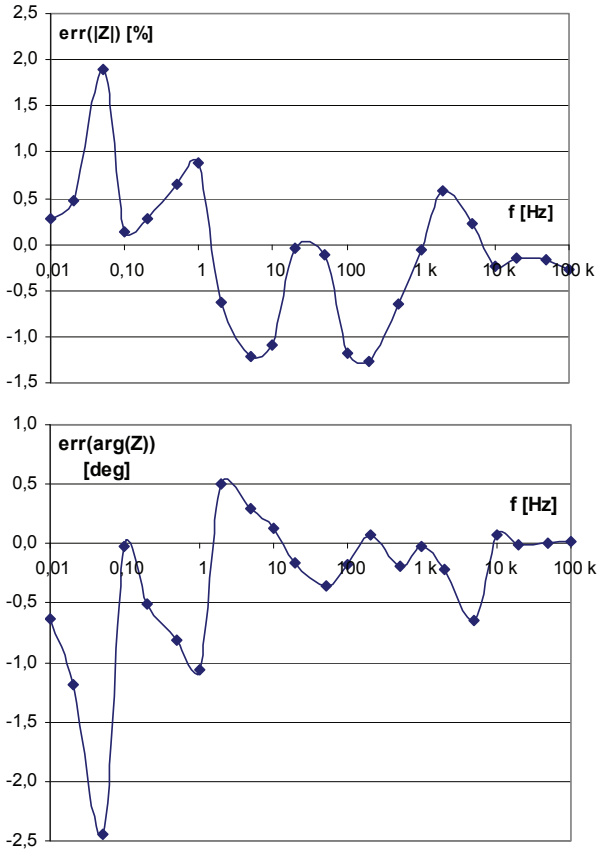

Fig. 8. Relative error of the impedance modulus and absolute error of impedance argument.

4. CONCLUSIONS

A portable analyzer for impedance spectroscopy of objects in the field has been developed. The impedance can be measured in the range of $10\,\Omega \le |Z_x| \le 10\,\mathrm{G}\Omega$ at frequencies in the range 0,01Hz ÷ 100 kHz (10 frequencies in each decade). In the construction of the analyser we propose a new solution based on two AD5933 specialized microsystems. This solution eliminates the disadvantages of the microsystem used in the configuration proposed by the manufacturer, e. g. the need of calibration measurement, too narrow range of measured impedance modulus 1 kΩ ÷ 10 MΩ and measurement frequency 1 kHz ÷ 100 kHz.

The performed tests of the realized prototype of the analyzer proved the achievement of the assumed parameters. The relative error of the impedance modulus is in the range of (+2 ÷ -1.3)% and the absolute error of the impedance argument (+0.5 ÷ -2.5)°, respectively. The meaningful dependence of errors on the measurement frequency in each decade of the generated measurement signals was observed. In the final version of the analyzer, when the additional programmed low-pass filter will be used, a decrease of the errors to ±1% and ±1° is expected.

The important advantage of the solution based on AD5933 microsystems is the decrease of power consumption down to ca. 0,5 W, what makes to power the measurement module directly from PC using +5 V from USB possible. It is a very profitable feature of the analyzer designed to work in the field.

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REFERENCES

[1] R. Bragos, R. Blanco-Enrich, O. Casas, J. Rosell, “Characterisation of Dynamic Biologic Systems Using Multisine Based Impedance Spectroscopy”, *IEEE Instrumentation and Measurement Technology Conference*, Budapest, Hungary, 2001.

[2] A. Carullo, M. Parvis, A. Vallan, “Fast impedance analyzer for corrosion monitoring”, *XVI IMEKO World Congress,* Vienna, Austria, vol. 6, 2000, pp. 161-165.

[3] K. Srinivas, P. Sarah, S. V. Suryanarayana, “Impedance spectroscopy study of polycrystalline BI6FE2TI3O18”, *Bulletin of Material Science*, vol. 26, 2003, pp. 247-253.

[4] H. Andersson, I. Petersson, E. Ahlberg, “Modelling electrochemical impedance data for semi-bipolar lead acid batteries”, *Journal of Applied Electrochemistry*, vol. 31, 2001, pp. 1-11.

[5] E. Angelini, A. Carullo, S. Corbellini, F. Ferraris, V. Gallone, S. Grassini, M. Parvis and A Vallan, “Handheld-impedance-measurement system with seven-decade capability and potentiostatic function” *IEEE Trans. On Instrumentation and Measurement*, vol. 55, No. 2, April 2006, pp. 436–441.

[6] Application Note AD5933 (Rev.0): 1 MSPS, 12-Bit Impedance Converter, Analog Devices 2005.