XIX IMEKO World Congress
Fundamental and Applied Metrology
September 6–11, 2009, Lisbon, Portugal

COMPARATIVE ANALYSIS OF DIFFERENT ACQUISITION TECHNIQUES APPLIED TO STATIC AND DYNAMIC CHARACTERIZATION OF HIGH RESOLUTION DAC

Domenico Luca Carnì, Domenico Grimaldi

Department of Electronics, Computer and System Sciences,
University of Calabria, 87036 Rende – CS, Italy
Ph.: +39 0984 494712, fax: +39 0984 494713, {dlcarni, grimaldi}@deis.unical.it

Abstract − Two acquisition techniques pointed out for the static and dynamic test of high resolution DAC by low resolution ADC are analyzed and compared. These two techniques differ on the basis of the specific approximated evaluation of the DAC output voltage.
The interest to the comparative analysis is justified by the aim to separate the influence of the acquisition technique from that of the processing algorithm on the evaluation of the accuracy of the test.
The comparing analysis is performed on the basis of the accuracy to reconstruct the output signal of the DAC. The error occurring in the evaluation of the DNL is taken into consideration for the static test. The error occurring in the evaluation of the Spurious Free Dynamic Range is taken into consideration for the dynamic test.
Results of the numerical tests to compare the accuracy of the two acquisition techniques are shown and discussed.

Keywords Digital to Analog Converter, Static test, Dynamic test, Sine fitting, Zero crossing.

1. INTRODUCTION

The characterization of high resolution Digital to Analog Converter (DAC) involves difficulties and problems caused by their high performance respect to the tradition ones [1], [2]. In particular, the acquisition system for both static and dynamic tests must be characterized by higher both resolution and linearity than that of the DAC under test.

Methods were proposed in literature for the static characterization [3]-[10] or the dynamic characterization [11]. Each one is based on particular procedures of the output signal from the DAC.

Only the two methods shown in [12]-[14] were pointed out to perform both the static and the dynamic characterization.

In [12] the problem of the acquisition system with high resolution and linearity is shifted to the problem of the generation of dithering signal by auxiliary DAC and the storage of large number of samples. Indeed, the large number of dither values corresponding to each acquired value are used to obtain, by difference with the ADC threshold level, the better approximation of the output of the DAC under test. Therefore, the samples used for the static and dynamic test are obtained by using the proper data processing algorithm.

In [13], [14] the problem of the signal acquisition with high resolution and linearity is shifted to the problem of the high speed acquisition at low resolution of the resulting signal sum of the DAC output and the reference signal. The reference signal, evaluated at the zero crossing sequence detected on the resulting signal, is used to reconstruct the DAC output. Also in this method an effective data processing algorithm guarantee the accurate evaluation of both the static and dynamic parameters.

Each one uses low resolution Analog to Digital Converter (ADC) to digitize the output signal from the DAC under test and auxiliary one.

The acquisition technique applied on each of these two methods differ according to the approach pointed out for the test. Consequently, the reconstruction procedure of the output signal of the DAC under test is different, also. The former is based on the processing of large number of data, the later is based on the processing of non uniformly sampled data.

In the paper, the acquisition technique of each of the two methods is taken into account and analyzed in order to compare the accuracy and the sensitivity to reconstruct the output signal of the DAC. The interest to this analysis is justified by the necessity to investigate about the influence on the evaluation of the accuracy and the sensitivity of each method by distinguishing the effects between the acquisition technique and the processing algorithm.

As concerns with the static characterization of the DAC, both the two acquisition techniques determine the output voltage of the DAC under test for all the possible input codes. Therefore, the evaluation of the Integral Non Linearity (INL) and Differential Non Linearity (DNL) are used for the comparing analysis. As concerns with the dynamic characterization, the DAC under test is forced to furnish the sinusoidal signal. Therefore, the modified version of the sine fitting algorithm, modified to be used in the case that the signal is sum of harmonics [15], is used for the comparing analysis.

ISBN 978-963-88410-0-1

The paper is organized as follows. In order to make it self containing, the two acquisition techniques are summarised. Successively, the aspects concerning with the comparing analysis and the modified version of the multi-sine fitting algorithm are presented. Finally, the results of the numerical tests to compare the accuracy and the sensitivity of each of two acquisition techniques are shown and discussed for the static and dynamic characterization of the DAC, separately.

2. TWO ACQUITION TECHNIQUES FOR HIGH RESOLUTION DAC

Fig.1 shows the block scheme of the test method based on the dithering signal and storage of large number of samples, proposed in [12]. For the static test, the PC feeds the DAC under test to generate the low frequency triangular waveform and the auxiliary DAC to generate the dithering signal. For the dynamic test, the DAC under test generates the sinusoidal signal.

Fig.2 shows the block scheme of the test method based on non uniformly sampled data, proposed in [13], [14]. For the static test, the PC feeds the DAC under test by means of the Digital Input Code DIC_k, k=0,…,2n-1, and the reference is the sinusoidal signal. For the dynamic test, the DAC under test generates the sinusoidal signal and the reference is the sawtooth signal.

The two methods use low-resolution ADC to digitize the signal obtained by summing the output signal of the DAC under test and the dithering or the reference signal.

The acquisition techniques of the DAC output voltage are different: (i) by processing the corresponding values of the dither signal and the ADC codes for the first method, and (ii) by means of the different zero crossing distribution in time of the resulting signal for the second method.

2.1. Static parameter estimation

For the static parameter estimation in [12] the transition levels of the DAC under test are estimated from the knowledge of the ADC output code obtained by any combination of the dithering signal and DAC output levels. The difference between any estimated ADC transition level and the dithering level furnishes the DAC output voltage. In particular, the DAC under test generates the triangular periodic waveform. During each period the dithering DAC will provide a distinct but constant dithering voltage. The ADC quantizes certain number of periods of the waveform with different dithering levels. Because of the different dithering levels, the ADC's output codes, associated with one output voltage of the DAC under test, are slightly different from that of the previous period.

In particular, the output code associated with a voltage right smaller than the ADC transition level will increase when the dithering level increases. The output codes of the ADC with the knowledge of the input code of the DAC under test and the voltage output of the dithering DAC are used to estimate:

- the ADC bin width using the constant interval of an output code of the ADC with constant value of the DAC under test and different values of the dithering DAC;
- the transition level of the ADC using the bin width;
- the output of the DAC under test as difference between the ADC transition level knowledge and the dithering DAC voltage output that causes the change of the ADC code.

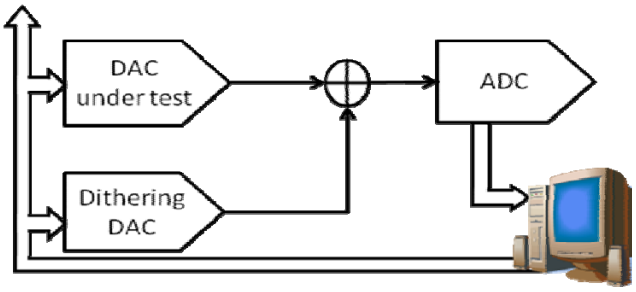


Fig.1. Testing equipment of the method based on the dithering signal.

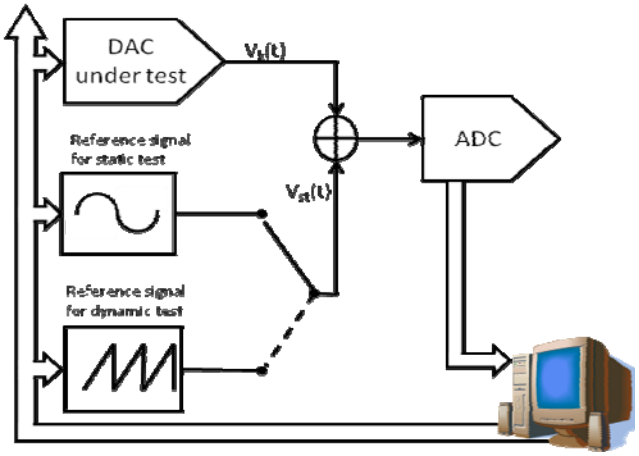


Fig. 2 Testing equipment of the method based on non uniformly sampled data.

The accurate evaluation of the output signal of the n bit DAC under test requires the acquisition on $2^n x 2^m$ samples, with m bit number of the auxiliary DAC.

The method proposed in [13] is based on the comparison of the output voltage signal v_k of the DAC under test with the reference one.

The resulting signal obtained by adding these two signals is oversampled by the high speed ADC. The Zero Crossing Time Sequence (ZCTS) detected into the resulting signal is used to infer the values of the reference signal and, consequently, the corresponding values of the output voltage of the DAC. In particular, the output voltage of the DAC under test is added to the sinusoidal reference voltage. The amplitude changes of the DAC output voltage are evaluated by means of the different zero crossing distribution in the time of the resulting signal. In fact, in the case of reference sinusoidal signal, the sequence in time between two successive zero crossings is characterised by only one constant time interval equal to the half-period. If the constant voltage v_k is added to the reference signal, the sequence in time

between two successive zero crossing changes, and two different time intervals were defined.

2.2. Dynamic parameter estimation

By sending the digital codes to generate sinusoidal waveform to the DAC under test, the methodology in [12] is used to test the dynamic performance. In this test the dither values corresponding to each acquisition time instant are considered to obtain the better approximation of the DAC output by the difference with the ADC threshold level. Each output voltage of the DAC must to be tested with every dither signal levels. This methodology requires the knowledge of the auxiliary DAC output voltage with high accuracy. In particular, knowledge error on the DAC output voltage causes error on the characterization of the DAC under test.

In [14] the DAC under test receives at the input the digital codes corresponding to the sinusoidal signal and the sawtooth signal is used as reference signal. These two signals are added and sent to the ADC. The ZCTS detected into the resulting signal is used to infer the values of the reference signal, and the corresponding values of the output voltage of the DAC. The ZCTS is non uniformly distributed in the time domain. Therefore, the reconstructed DAC output signal is characterised by non uniform sampling.

3. COMPARING ANALYSIS OF THE TWO ACQUITION TECHNIQUES

The two acquisition techniques distinguish they self on the basis of the specific approximated evaluation of the DAC output voltage, both for the static and the dynamic characterization. Consequently, the comparing analysis must be based on common processing procedure in order to evaluate the accuracy and the sensitivity to reconstruct the output signal of the DAC.

As concern with the static characterization of the DAC, both the acquisition techniques determine the output voltage of the DAC under test for all the possible input codes. Therefore, the comparing analysis of the acquisition techniques is carried out by evaluating the Integral Non Linearity (INL) and the Differential Non Linearity (DNL) [16], [17].

In particular, once assigned in simulation environmental to the DAC the previous established DNL, the absolute error is evaluated between the DNL estimated and that imposed.

As concern with the dynamic characterization, the comparing analysis is carried out by evaluating the accuracy for the reconstruction of the output signal of the DAC. In order to make the evaluation independent from the algorithm, the multi-sine fitting algorithm [15], [18] is used to process the data furnished by each of the two acquisition techniques.

The input data to this algorithm are the amplitude of the acquired signal and the sampling time. It is not influenced by the non uniform sampling. It is the modified version of the sine fitting algorithm to be used in the case that the signal is sum of harmonics.

In particular, it starts by evaluating the coarse initial values of the frequency, amplitude, phase and offset. Fig.3 shown the block scheme of the procedure pointed out to evaluate the coarse initial values. The coarse evaluation of initial value of the harmonic parameters is performed in two steps. In the former the initial value f_0 of the frequency of the fundamental harmonic is estimated. This estimation is based on the evaluation of the semi-period of the signal reconstructed by the acquisition technique. In the latter the initial value of amplitude and phase of the harmonics, and the dc offset are estimated. The estimation is performed by using the MSFA based on the three parameters sine-fitting, once the number of harmonics is established. Once estimated the parameter coarse values, the MSFA based on the four parameters sine-fitting is used to evaluate the accurate final values. The iterations of the MSFA stop when the frequency change is suitably small.

The results of the four parameters multi-sine fitting algorithm can be used to characterize the dynamic behaviour of the device by means of Total Harmonic Distortion (THD) and Spurious Free Dynamic Range (SFDR) and Signal to Noise Ratio (SNR).

A problem in the MSFA based on four parameters sine fitting is the evaluation of the initial condition of the fundamental harmonic frequency, amplitude and phase of each harmonic to ensure the convergence. The convergence is not assured for each value of the initial conditions. Indeed, it is highly dependent on the initial frequency and the number of samples used [15]. If the algorithm converges, the number of iterations is highly dependent on the initial conditions. Moreover, it can converge to local minimum instead of the global one.

To overcome this problem, in [16] has been proposed a proper and efficient technique that permit to evaluate the initial condition for ensuring the convergence of the MSFA.

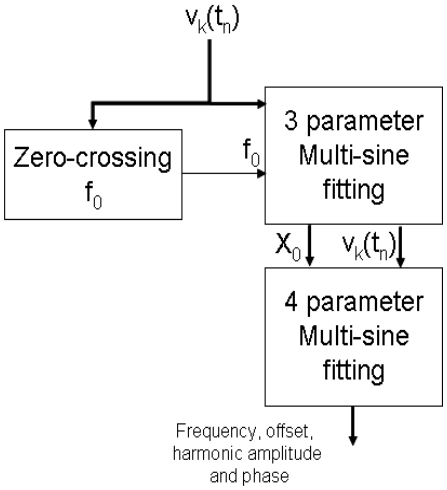


Fig. 3 Block scheme of the procedure pointed out to evaluate the coarse initial values of the harmonics, and their accurate and final values.

4. NUMERICAL TEST

Numerical tests are performed in Matlab environment to analyse and to compare the accuracy and the sensitivity of each of the two acquisition techniques.

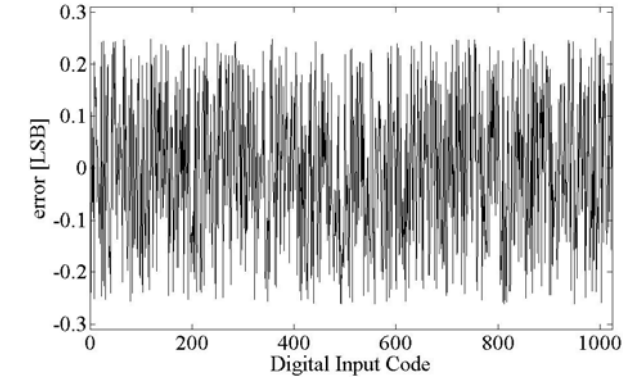
The numerical results shown in the following refer to 10 bit resolution DAC and 8 bit resolution ADC.

4.1. Static test comparison

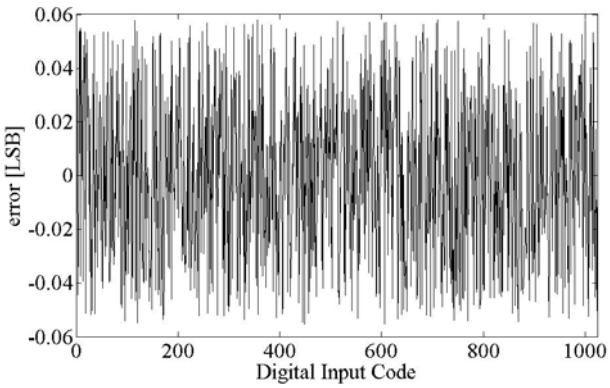
As concern with the static test, the comparing analysis is based on the evaluation of the reconstruction accuracy of the alterations imposed to the DAC levels by means of the DNL.

The non ideality of the DAC is simulated by imposing the DNL into the range [-3.00, +3.00] LSB. In particular, each output value of the DAC corresponding to assigned input code is altered by summing the corresponding value of the DNL. Moreover, to simulate other noise source, at the output voltage is added Gaussian noise with maximum amplitude equal to 0.1LSB**.**

For the first acquisition technique is considered the dithering with amplitude equal to 3LSB. For the second acquisition technique is considered the sinusoidal reference signal with frequency equal to 1kHz and amplitude equal to 1.5 times the full-scale voltage of the DAC, according to the theoretical and experimental results shown in [13]. The sampling frequency of the ADC is set equal to 50MS/s.



a)



b)

Fig. 4 Error trend for the DNL estimation by referring to 10 bit DAC, in the case of method a) based on the storage of large number of samples, and b) based on non uniformly sampled data.

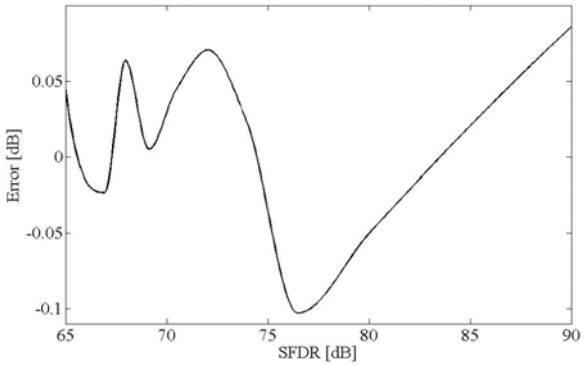


Fig. 5 Error trend in the SFDR evaluation versus the assigned SFDR value in the case of the method based on non uniformly sampled data.

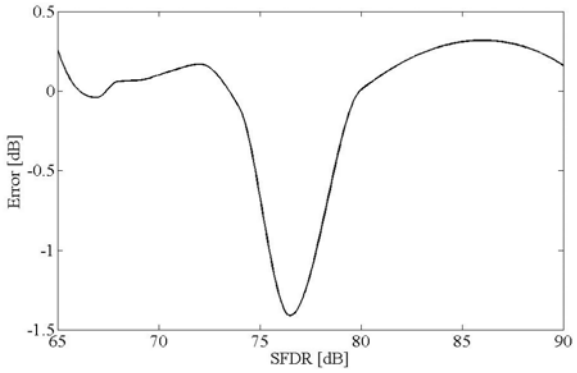


Fig. 6 Error trend in the SFDR evaluation versus the assigned SFDR value in the case of the method based on the dithering signal and storage of large number of samples

The absolute error between the DNL estimated and the DNL imposed are shown in Fig.4 for both the methods. The DNL error estimation is in the range [-0.25, 0.25]LSB for the method based on the dithering signal and storage of large number of samples (Fig.4a). For that based on non uniformly sampled data, the absolute error is included in the range [-0.06, 0.06]LSB corresponding to the superimposed Gaussian noise (Fig.4b). As a conclusion, the second method guaranties better accuracy than the first one.

4.2. Dynamic test comparison

For the comparing analysis of the acquisition techniques in the case of dynamic test, the error is estimated by referring to the evaluation of the SFDR.

In particular, Fig.5 shows the error trend for the SFDR evaluation versus the assigned SFDR value in the case the method based on non uniformly sampled data is taken into account. Fig.6 shows the error trend for the SFDR evaluation versus the assigned SFDR value in the case the method based on the dithering signal and storage of large number of samples is taken into account.

Fig.5 and Fig.6 highlight that the method based on non uniformly sampled data guaranties the error in the SFDR estimation lower than 0.1 dB. Differently, the method based on the dithering signal and storage of large number of samples shows the error lower than 1.5 dB.

On the basis of these results, the method based on non uniformly sampled data shows lower error, therefore in the following their sensitivity is analysed.

Fig.7 shows the trend of the percentage error in the fundamental harmonic estimation versus the assigned value of fundamental harmonic. It shown as the percentage error decrease with the increasing of the sinusoidal signal amplitude. The test is performed by (i) considering that the other harmonics have amplitude equal to the noise floor, and (ii) processing 200 samples. This number of samples is established according to the results shown in [23], that highlight as the percentage error in the SFDR estimation do not decrease with the increasing of the processed samples higher than 200. In fact, the multi-sine fitting method approximates the sampled signal in the time domain by the constant number of sinusoids independently from the number of samples processed.

4. CONCLUSIONS

The comparing analysis of two acquisition techniques pointed out for the static and dynamic test of high resolution DAC is performed.

These two techniques use low resolution ADC, but distinguish they self on the basis of the specific approximated evaluation of the DAC output voltage.

On the basis of this diversity can be justified the different accuracy shown to reconstruct the output signal of the DAC and highlighted by the numerical results presented in the paper.

As concern with the comparing analysis for the static test, the reconstruction error of the alterations imposed to the DAC levels by means of the DNL is evaluated.

As concern with the dynamic test, the error occurring in the evaluation of the Spurious Free Dynamic Range is evaluated.

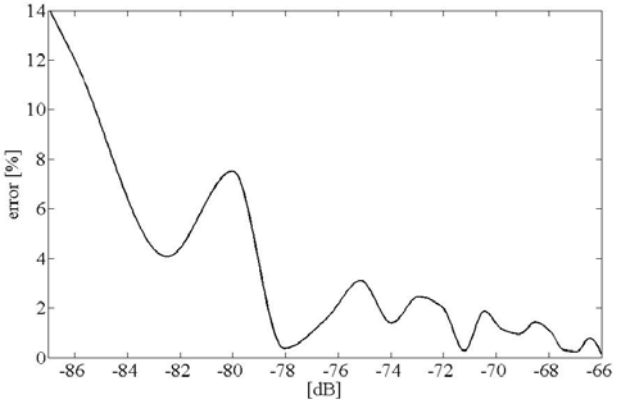


Fig. 7 Error trend in the fundamental harmonic evaluation versus the assigned value of the fundamental harmonic for the of the method based on non uniformly sampled data.

The interest to the analysis is justified by the aim to separate the influence of the acquisition technique from that of the processing algorithm on the evaluation of the accuracy of the test.

REFERENCES

[1] E. Balestrieri, P. Daponte, S. Rapuano, "Recent development on DAC modelling testing and standardization", Measurement, vol. 39, No.3, April 2006, Pages 258-266.

[2] International Technology Roadmap for Semiconductor, 2003 edition, available online at http://public.itrs.net.

[3] T.M. Souders, G.N. Stenbakken, "A comprehensive approach for modeling and testing analog and mixed-signal devices", Proc. of IEEE ITC 90, Washington, USA, September 1990, pp. 169–176.

[4] P.P. Fasang, "An optimal method for testing digital to analog converters", Proceedings of the 10th IEEE Int. ASIC Conf. and Exhibit, Portland, USA, Sept.1997, pp. 42–46.

[5] A. Wrixon, M.P. Kennedy, "A rigorous exposition of the LEMMA method for analog and mixed-signal testing", IEEE Trans. on Instr. and Meas., vol.48, No.5, 1999, pp. 978–985.

[6] Analog Device, Inc., "Analog-Digital Conversion Handbook", D.H Sheingold, Ed. Englewood Cliffs, NJ: Prentice-Hall, 1986.

[7] B. Vargha, J. Schoukens, Y. Rolain, "Using reduced-order models in D/A converter testing", Proc. of the 19th IEEE Instr. and Meas. Tech. Conf., Anchorage (USA), 21-23 May 2002, vol.1, pp. 701-706.

[8] Y.C. Wen, K.J. Lee, "BIST structure for DAC testing", Electr. Letters, 11th June 1998, vol.34, No.12, pp 1173-1174.

[9] I.H.S. Hassan, K. Arabi, B. Kaminska, "Testing digital to analog converters based on oscillation-test strategy using sigma-delta modulation", Proc. of the Intern. Conf. on Computer Design ICCD, 1998, pp40-46.

[10] S.J. Chang, C.L. Lee and J.E. Chen, "BIST scheme for DAC testing", Electronic Letters, 18th July 2002, vol. 38, No.15, pp 776-777.

[11] J. Savoj, Ali-Azam Abbasfar, A. Amirkhany, B.W. Garlepp, M.A. Horowitz, "A new technique for characterization of Digital-to-Analog Converters in high-speed systems" Design, Automation & Test in Europe Conf.& Exhibition, , 16-20 April 2007, pp.1-6.

[12] J. Le, H. Hosam, R. Geiger, C. Degang, "Testing of precision DACs using low-resolution ADCs with dithering", Proc. of IEEE Intern. Test Conf., Oct. 2006, pp.1-10.

[13] D.L. Carnì, D. Grimaldi, "Static characterization of high resolution DAC based on over sampling and low resolution ADC", Proc. of IEEE Instrum. and Measur. Techn. Conf., I2MTC 2007, Warsaw, Poland, May 1-3, 2007.

[14] D.L. Carnì, D. Grimaldi, "Over sampling method for the static characterization of high resolution DAC: a proposal for the IEEE Standard P1658", Proc. of IMEKO 12th Workshop on ADC, Iaşi – Romania, Sept.19-21, 2007.

[15] P.M. Ramos, M. Fonseca da Silva, R.C. Martins, A.M.C. Serra, "Simulation and Experimental Results of Multiharmonic Least-Squares Fitting" IEEE Transactions on instr. and Meas., Vol. 55, N 2, April 2006, pp. 646 – 651.

[16] D.L. Carnì, G. Fedele, "Improved evaluation of initial condition for the multi-sine fitting algorithm", IDAAC 2009.

[17] E. Balestrieri, S. Moisa, S. Rapuano, "DAC static parameter specifications – some critical notes", Proc. of 10th IMEKO TC-4 Work. on ADC Modelling and Testing, Gdynia and Jurata (Poland), Sept. 12-15, 2005, vol. I, pp.81-86.

[18] E.Balestrieri, S. Rapuano, "Defining DAC performance in the frequency domain", Meas., vol. 40, No.5, June 2007, Pages 463-472.

[19] D.L. Carnì, D. Grimaldi, "'Characterization of High Resolution DAC by DFT and Sine Fitting" I2MTC, Singapore, May 5-7, 2009.