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SIGNATURE TESTING OF ANALOG-TO-DIGITAL CONVERTERS

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Abstract – When testing an analog-to-digital converter (ADC) by automatic test equipment (ATE), the latter is capable of performing extensive processing of output responses of the ADC. This allows detection of virtually any fault. However, the cost of ATE is quite high. As well, the external bandwidth of ATE is normally lower than the internal bandwidth of the ADC being tested, which makes it difficult to accomplish at-speed testing. It is important, therefore, to embed test hardware into ADC itself. The methods employed at ATE are complex and inconvenient for built-in realization. More advantageous are the methods exploiting accumulation of output responses. The size of the accumulator depends on the number of responses. In order to achieve greater fault coverage, this number is kept large, complicating the implementation. On the other hand, signature analysis used in digital systems testing is well suited for compaction of "lengthy" responses, and it is characterized by small hardware overhead and low aliasing probability. In this work, we apply signature analysis principle for compaction of output responses of an ADC. The permissible tolerance bounds for a fault-free ADC are determined and the aliasing rate is estimated. Examples are given.

Keywords: analog-to-digital converter, built-in self-test, signature analysis

1. INTRODUCTION

Analog-to-digital converters are primary units of mixed-signal systems that are responsible for the overall accuracy. These systems (e.g. measurement systems) may contain few ADCs and a common processing part implemented on a programmable device(s) [1]. Various ADCs are the essential part of many applications utilized in industry and research. Thus, their improper operation must be detected as soon and as efficiently as possible. ADCs are characterized by two possible types of failures: sudden failures and gradual failures. Gradual failures represent greater danger, since they may remain hidden over a long period of time.

To be efficient, test hardware must be small and it must provide for low aliasing rate. Signature analysis has been digital systems testing technique that perfectly satisfies these requirements. In this method, inputs of a digital device under test (DUT) are fed by the sequence of test stimuli (normally exhaustive), whereas the output responses are compacted into a signature. The signature is compared with the one for the fault-free device. Their mismatch indicates that the DUT is faulty.

Feeding inputs with the exhaustive sequence of stimuli increases fault coverage, but compaction of the output response causes some errors to escape detection due to aliasing. With the size of signature equal to 16, the aliasing rate is sufficiently low, such that the efficiency of the method is quite high. Because of these attractive features, signature analysis has gained considerable popularity. We will attempt to use similar technique for testing of ADCs.

As applied to an ADC, exhaustive sequence of stimuli would include an infinite number of analog signals covering the full scale range. In practice, this number is limited to the characteristic points of the range. If ADC is a part of the measurement system that is intended to convert an active value (such as voltmeter), the test sequence can be generated on-chip by various types of precise waveform generators [2]-[4]. In the case of a system converting passive parameters (such as impedance meter), the input stimuli can be produced by high precision resistors and capacitors [5].

The methods of output response compaction for mixed-signal systems can roughly be divided into two groups. The first group is based on extensive processing of the responses with further extraction and evaluation of the characteristic static or dynamic parameters of the transfer function of the system [2]-[8]. These methods involve a computing device and are complex for on-chip realization.

The second group of methods is based on the estimation of the sum of the output words (vectors) [9], [10]. For the *n*-bit ADC, the method requires a *2n*-bit adder. In order to increase fault coverage, the number of test patterns (points) must be large enough. This significantly increases the size of the adder required. Obviously, compaction of the sum would save test hardware. The widely used method of compaction of digital data, signature analysis, is not applicable here, because of unavoidable quantization error existing in the conversion results. In error-control coding, situations like this are remedied by arithmetic (residue) codes, namely the modulo sum method. We will use this method for ADC response compaction referring to the residue as signature. We will also estimate the fault free circuit signature bounds and the aliasing rate for the case when all errors in the output words are independent.

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2. PROBLEM STATEMENT AND TESTING METHOD

A multi-channel measurement system (MS) is represented in Figure 1 [11]. It consists of r channels (ADCs), $Ch_1,...,Ch_r$, a microcontroller unit, *MCU*, and waveform generators, $WG_1,...,WG_r$. The inputs of the MS are fed either by signals being measured, $x_1,...,x_r$, or test (reference) stimuli, $x_1^0,...,x_r^0$, through the multiplexors.

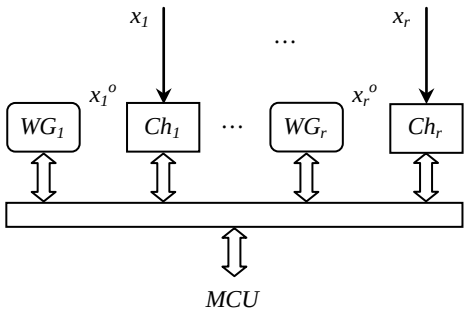

Fig. 1. A multi-channel measurement system.

The transfer characteristic of the ideal (and fault-free) ADC, whose full scale range, $FSR = 8V$, is shown in Figure 2 [11]. For a real fault-free ADC, the transitions between steps may fluctuate within the permissible tolerance bounds, $k - 1 < T(k) < k$, where $T(k)$ is the k-th transition voltage, $k = 1,\ldots,2^n - 1$; and n is the resolution of the ADC (the number of bits in the output code). These bounds are shown by dotted lines surrounding the ideal transitions. If we could apply a very precise voltage, e.g. $4V$, to the input of the ADC, the output code would be 100_2. However, the voltage that normally comes from the on-chip waveform generator is not accurate. The problem is aggravated with the continued growth of the resolution of modern ADCs,

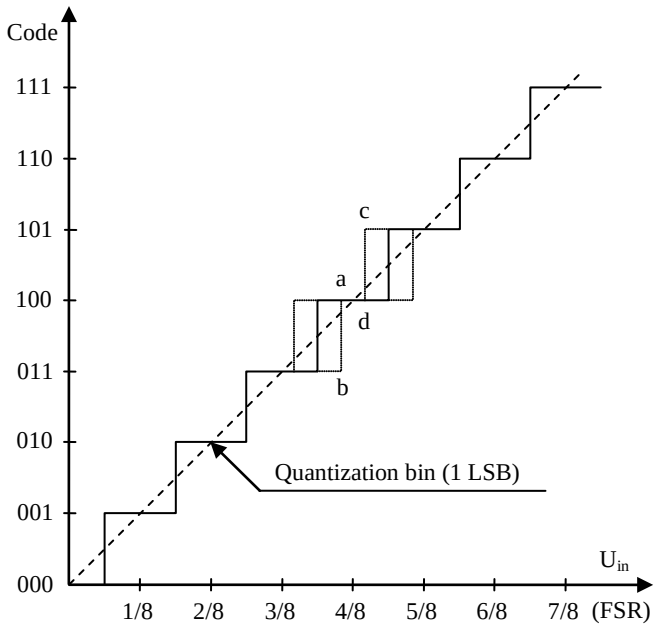

Fig. 2. The transfer characteristic of the ideal 3-bit ADC with FSR=8V.

resulting in the contraction of the quantization bin. Hence, the real test voltage (stimuli) becomes an interval value. Note that the rightmost permissible value for the transition $T(k)$ and the leftmost permissible value for the transition $T(k + 1)$ (e.g. points a and d in Figure 2, $k = 4$) lie in the infinitesimal neighborhood of the middle point of the corresponding quantization bin. If an interval voltage that covers the middle point is applied to the ADC, it will also produce an interval code, even though no faults are present. For the $4V$ input voltage, the permissible output codes will be 011, 100, and 101. This uncertainty complicates the use of algebraic compaction for ADCs testing.

Using the same approach, we can observe that the voltage, U_{in}, belonging to the interval $|U_{in} - 3.5| < 0.5$, and applied to the same ADC, will produce only two permissible codes: 011 and 100. However, as we will see further, if the inputs of the ADC under test are fed by the stimuli that match the ideal transition voltages, the aliasing rate will not change notably.

It can also be noticed that refining the accuracy of the input voltage beyond 0.5 LSB does not reduce the output uncertainty and, therefore, is not required. This relaxes the accuracy requirements for waveform generators.

Failure in the analog part of the ADC may change positions of the transition points beyond the permissible bounds, influencing the widths of the quantization bins. When two consecutive transition edges move toward each other the width becomes zero. If this happens for a few adjacent quantization bins, there will be a sudden (exceeding unity) change in the output code. Similar behavior would be observed, if failures had occurred in the digital part. Irrespective of the nature of failure, we will select the following criterion to test the operability of an ADC. If the output code of an ADC fed by a test voltage exceeds the expected (permissible) tolerance bounds which were defined above, the ADC will be assumed faulty.

We will only consider testing of a single channel, as the other channels are tested similarly. Therefore, the channel index will be dropped. Let m be the number of distinct values of the signal x^o which are sufficient to detect all faults that may occur in the channel in question. And let x_i^0 be the value of x^o at time t_i. Then, the actual output code corresponding to the input value x_i^0 will be $y_i = [x_i^0 + 0.5q] + \delta_i = y_i^0 + \delta_i$, $i = 1,\ldots,m$. Here q is the width of the quantization bin (equal to $1V$ in Figure 1); $[a]$ represents the integer part of a; y_o is the ideal output code; and δ_i is the actual static error.

We will denote the permissible upper and lower tolerance bounds as $\bar{\delta}_i$ and $\underline{\delta}_i$, $i = 1,\ldots,m$. For a fault-free ADC the following inequalities are satisfied: $\underline{\delta}_i \le \delta \le \bar{\delta}_i$, $i = 1,\ldots,m$. From the standpoint of practical realization, it is more convenient to verify the equivalent conditions, $\underline{y}_i \le y \le \bar{y}_i$, where $\underline{y}_i = y_i^0 + \underline{\delta}_i$, $\bar{y}_i = y_i^0 + \bar{\delta}_i$.

Similar to the principle used in a multiple-input signature analyzer, we will compress all output codes of the ADC into one signature. But in contrast to the algebraic addition with respect to a characteristic polynomial, we will perform arithmetic addition modulo $L = 2^n$, where n is the resolution

of the ADC being tested. After adding up all the codes, the final sum will be:

$$\sum_{i=1}^{m} y_i = \sum_{i=1}^{m} y_i^0 + \sum_{i=1}^{m} \delta_i,$$

Using the notations

$$Y = \sum_{i=1}^{m} y_i,\ Y^0 = \sum_{i=1}^{m} y_i^0,\ \Delta = \sum_{i=1}^{m} \delta_i$$

we will obtain $Y - Y^0 = \Delta$. Here Y^0 can be calculated based on the ideal transfer characteristic of the ADC. It has the same value regardless of the actual (faulty or fault-free) state of the ADC.

Since we consider symmetrical ADCs, then $\breve{\delta}_i = \breve{\delta}$, $\hat{\delta}_i = \hat{\delta}$ for every *i = 1,…,m*. Taking this into account and introducing the following bounds:

$$\breve{\Delta} = (\sum_{i=1}^{m} \hat{\delta}_i) \bmod L, \quad \hat{\Delta} = (\sum_{i=1}^{m} \breve{\delta}_i) \bmod L$$

it can be shown that the ADC will certainly be faulty, if the following condition holds:

$$m\hat{\delta} < (Y - Y^0) \bmod L < L - m\left|\breve{\delta}\right| \tag{1}$$

Otherwise, we will assume that the ADC is fault-free. Here the residue $R = (Y - Y^0) \bmod L$ is the actual signature. Therefore, the fault free circuit signature must belong to one of the intervals: $[0, \breve{\Delta}]$, or $[\hat{\Delta}, L-1]$.

Computation of the residue *R* is performed in the adder that is preliminary loaded with the seed value, namely the two's complement of Y^0. The two's compliment is defined as $\bar{Y}^0 = -Y^0 \bmod L$. Equation (1) will then have the form:

$$m\hat{\delta} < (Y + \bar{Y}^0) \bmod L < L - m\left|\breve{\delta}\right| \tag{2}$$

Example 1 The offset of the fault-free ADC is 0. Let us consider the 8-bit ADC, whose offset has become +2 (FSR/256) due to a failure. The ADC is fed by the five test stimuli, x_1^0 = 201/256 FSR, x_2^0 = 202/256 FSR, x_3^0 = 203/256 FSR, x_4^0 = 204/256 FSR, x_5^0 = 205/256 FSR. Let the actual readings of the ADC be accordingly: $y_1^0 = 203$, $y_2^0 = 203$, $y_3^0 = 205$, $y_4^0 = 207$, $y_5^0 = 206$. Here *m*=5, *n*=8, $\hat{\delta} = \left|\breve{\delta}\right| = 1$, Y =1024; Y^o=1015; $\bar{Y}^0$=9, $\breve{\Delta}$ =5, $\hat{\Delta}$ =251. And condition (2), 5 < (1024 + 9) mod 256 < 251, is satisfied. Therefore, the failure is detected. If the offset were 0, then *Y* would have been 1014. And condition (2) would not hold: 5 < 255 > 251!

3. ALIASING

Aliasing occurs when the signature of a faulty circuit matches the signature of the fault-free circuit. The aliasing rate for an ADC can be estimated as the ratio of the number of all undetectable errors in the output response of the ADC to the number of all possible errors in that response.

Let us first estimate the aliasing rate for the ideal ADC. The output response stream consists of $m \times n$ bits that are going to be compacted into *n* bits. It can be shown that under these conditions the aliasing rate will be $P_{ADC/idl} = (2^{(m-1)n} - 1) / (2^{mn} - 1)$. In most practical cases, $P_{ADC/idl} \approx 2^{-n}$. If the ADC is replaced by a purely digital circuit, this estimate remains true. Therefore, the aliasing rate for the digital system being tested by modulo sum method is $P_{dgt} = P_{ADC/idl} \approx 2^{-n}$.

It can be shown that for a real ADC, the aliasing rate becomes

$$P_{ADC} = \frac{2^{(m-1)n} - (\left|\breve{\delta}\right| + \left|\hat{\delta}\right| + 1)^m}{2^{mn} - (\left|\breve{\delta}\right| + \left|\hat{\delta}\right| + 1)^m} \tag{3}$$

Under certain conditions, we can obtain $P_{ADC} \approx 2^{-n}$.

Example 2 For the ADC considered in Example 1, equation (3) yields $P_{ADC} \approx 0.0039$.

For an arbitrary choice of *m* and *n*, equations (2) and (3) will have the forms:

$$m < (Y + \bar{Y}^0) \bmod L < -m \bmod L \tag{4}$$

$$P_{ADC} = \frac{2^{(m-1)n} - 3^m}{2^{mn} - 3^m} \tag{5}$$

If the input of an ADC is fed by the stimuli matching the ideal transitions of the transfer characteristic, then expressions (2) and (3) are simplified to:

$$0 < (Y + \bar{Y}^0) \bmod L < -m \bmod L \tag{6}$$

$$P_{ADC} = \frac{2^{mn-m-n} - 1}{2^{mn-m} - 1} \tag{7}$$

And if $mn >> (m + n)$, then $P_{ADC} \approx 2^{-n}$.

Comparing (5) and (7) we can observe that for practical values of *m* and *n*, the aliasing rates for these two cases are almost the same and equal to 2^{-n}. The aliasing rate decreases with the growth of the resolution of an ADC. As an alternative, the size of the modulo adder can be increased, if the resolution can not be raised further. It can also be noticed that under these conditions the aliasing rate does not change with the further increase of *m*. This is only accurate, if errors in the output stream are equally likely. In real ADCs these errors are correlated, therefore the estimates given can be considered as a first approximation.

4. CONCLUSION

We considered an output response compaction method which can be used for built-in self-test of analog-to-digital converters. The method implies feeding the ADC with analog test stimuli and evaluating the result of the compaction of the output responses, referred to as signature. If the signature does not hit a predefined interval, the ADC is considered to be faulty. The tolerance bounds for the signatures of the fault-free channels are evaluated. It is shown that these bounds depend on the input stimuli. The aliasing rate is estimated. Two sets of the input stimuli are examined. It is demonstrated that under an independent error model, the aliasing rate for these two sets is equivalent, and it does not change noticeably with the increase of the number of input stimuli. However, it does change when the resolution of the ADC being tested (or the length of the signature) is altered. The aliasing rate is reduced with the growth of the resolution.

In the case of a direct-conversion ADC with an intermediate conversion of the measured electrical value into time, implementation of the method is fairly simple. The binary counter used in such an ADC is utilized as a signature compactor. In the testing mode, it is reset not after each conversion, but only after a series of conversions for the entire sequence of test stimuli. The counter is preliminary loaded with the seed value, and after the series of conversions it contains the actual signature.

To further increase sensitivity of a signature to special types of errors at the output response of the ADC, we can select the compaction modulo in the form of $L_p = 2^n - 1$. The compactor will now detect all single errors [12].

Practical implementation of the method is facilitated in the systems measuring frequency dependant parameters (such as impedance). In these systems the test stimuli can be obtained by deviation of the frequency of the current that feeds the impedance being measured. This will significantly lower test hardware overhead, although it may increase the correlation rate between failures.

The technique considered in this work can also be used for the compaction of signals at test points of an analog circuit by means of a precise (and fault-free) ADC. The only difference in the reasoning is that the interval of permissible tolerance bounds will now be wider. The bounds will consist of two components, one being dependant on the ADC and the other being dependant on the analog circuitry that is responsible for the analog signal.

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REFERENCES

[1] V. Kneller, "Measurement, control and other processes: to the problem of knowledge systematization", *XVII IMEKO World Congress*, pp. 1119-1124, Cavtat-Dubrovnik, Croatia, June 2003.

[2] Y.-S. Wang, J.-X. Wang, F.-C. Lai and Y.-Z. Ye, "A low-cost BIST scheme for ADC testing", *VI Int. Conf. on ASIC*, vol. 2, pp. 665-668, Shanghai, China, October 2005.

[3] D. Lee, K. Yoo, K. Kim, G. Han and S. Kang, "Code-width testing-based compact ADC BIST circuit", *IEEE Trans. on Circuits and Systems-II: Express briefs*, vol. 51, nº 11, pp. 603-606, Nov. 2004.

[4] G. Wu, J. Rao, A. Ren and M. Ling, "Implementation of a BIST scheme for ADC test", *V Int. Conf. on ASIC*, vol. 2, pp. 1128-1131, Beijing, China, October 2003.

[5] A. Gookin, "A fast reading high resolution voltmeter that calibrates itself automatically", *Hewlett Packard J.*, vol. 28, nº 6, pp. 2-10, February 1977.

[6] A. Serra, "On the static test of Analogue-to-Digital Converters", *49th Int. Midwest Symposium on Circuits and Systems*, vol. 2, pp. 315-318, San Juan, Puerto Rico, August 2006.

[7] S. Mohan and M. Bushnell, "A code transition delay model for ADC test", *14th Int. Conf. on VLSI Design*, pp. 274-282, Bangalore, India, January 2001.

[8] G. Muginov and A. Venetsanopoulos, "A new approach for estimating high-speed analog-to-digital converter error", *IEEE Trans. on Instrumentation and Measurement*, vol. 46, nº. 4, pp. 980-985, August 1997.

[9] G. Roberts, "Metrics, techniques and recent developments in mixed-signal testing", *IEEE/ACM Int. Conf. on Comp. Aided Design*, pp. 1-8, San Jose, USA, November 1996.

[10] C. Stroude, J. Morton, T. Islam and H. Alassaly, "A mixed-signal built-in self-test approach for analog circuits", *Southwest Symp. on Mixed-Signal Design*, pp. 196-201, February, Las Vegas, USA, 2003.

[11] G. D'Antona and A. Ferrero, *Digital Signal Processing for Measurement Systems*, Springer Science + Business Media Inc., Berlin, 2006.

[12] J. Wakerly, *Error Detecting Codes, Self-Checking Circuits and Applications*, Elsevier North-Holland, New York, 1978.