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A 3 BITS DISCRETE PURE LINEAR ANALOG PREPROCESSING FOLDING ADC ARCHITECTURE BASED ON CASCADE CONTROLLED CHANNELS

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Abstract – A very simple circuit for a 3-bits discrete pure linear analog preprocessing folding ADC is presented. The device is based on the folding idea: the DAC, the summing node and the amplifier, fundamental elements of the classical architecture, are eliminated and replaced with an analogical signal preprocessing parallel structure named "channels". All channels are connected as a cascade and only three transistors constitute each one. The circuit has been widely analyzed by simulation and its simplicity guarantees easiness of realization, reduction of power consumption and reduction of total conversion time, making it close to the ADC flash. A first discrete circuit it has been realized and tested.

Keywords: ADC, folding, preprocessing analog channels.

1. INTRODUCTION

The demand of analog to digital converters (ADC), joined with the use of digital systems, is constantly growing.

An overwhelming variety of ADCs exist on the market today, with differing resolutions, bandwidths, accuracies, architectures, packaging, power requirements, and temperature ranges, as well as hosts of specifications, covering a broad range of performance needs. And indeed, there exists a variety of applications in data acquisition, communications, instrumentation, and interfacing for signal processing, all having a host of differing requirements.

Considering architectures, for some applications just about any architecture could work well; for others, there is a "best choice". In some cases the choice is simple because there is a clear-cut advantage to using one architecture over another [1].

In the field of very high speed, the flash ADC remains dominant. A set of 2^n–1 comparators is used to directly measure an analog signal to a resolution of n bits. For a 4-bit flash ADC, the analog input is fed into 15 comparators, each of which is biased to compare the input to a discrete transition value. These values are spaced one least-significant bit apart. The comparator outputs simultaneously present 2^n–1 discrete digital output states. Together, these outputs can be read much like a liquid thermometer. The final step is to level-decode the result into binary form.

The disadvantage of this approach is that it requires a large number of comparators that are carefully matched and properly biased to ensure that the results are linear. Since the number of comparators needed for an n-bit resolution ADC is equal to 2^n–1, limits of physical integration and input loading keep the maximum resolution fairly low.

Subranging converters achieve higher resolutions than flash converters containing a similar number of comparators. This comes at the price of reducing of speed and bandwidth.

The folding is a version of the subranging architecture [2,3]. By an analog preprocessing circuit in folding A/D converters the number of comparators can be reduced significantly. Folding architecture reduces the total conversion time than a classical subranging [1].

In this paper, a simplified linear folding architecture for subranging ADC is presented. The preprocessing analog structure is constituted with 2^n (with n number of bits) parallel circuits made with a simple subtracting node and with a series of two mos switches able to join the functionalities of the DAC, the summing node and the amplifier typical of classical subranging ADC. After accurate simulation of the singles channels and of the whole structure, a first discrete circuit it has been realized and tested to validate the idea.

2. CLASSIC SUBRANGING AND LINEAR FOLDING ADC

The subranging ADC architecture dominates today's applications where sampling rates of greater than 5 MSPS to 10 MSPS are required. Although the flash architecture dominated the market in the 1980s and early 1990s, the subranging architecture has largely replaced the flash ADC in modern applications. This architecture was first used in the 1950s as a means to reduce the component count and power of the flash ADCs. For this architecture there are two principal implementations: the two-steps and the folding [4].

The two-steps A/D converter gets efficiency by dividing an *N*-bits quantization into lower-resolution quantization. In such a converter the first n_1-bits quantizer called "coarse" digitizes the input signal with low resolution, and applies the resultant MSBs to the reconstruction DAC. The analog output of the DAC is subtracted from the original input to form a residue signal, which is quantized by an n_2-bits quantizer, generating the lasts LSBs of the total n_1+n_2 output word. This approach gives good advantage because the

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combined complexity of the n_1-bit coarse and the n_2-bit fine quantizers can be very low, compared with the complexity of a single *N*-bits quantizer.

The target of a folding A/D converter is to form the residue signal with simple analog circuits, thereby obviating the need for the coarse quantizer, the DAC, and the subtracter of subranging ADC. In such an implementation (figure 1a), the low dynamic-range residue signal generated by the analog folding circuit directly drives the fine quantizer. However, because of the periodic nature the residual signal, the digitized output from the fine quantizer is ambiguous, and coarse quantizer is still necessary to ascertain in which period of the folding circuits transfer characteristic the quantizer input signal lies. This ADC can best be analyzed by examining the residue waveform at the input to the second-stage ADC as shown in Figure 2.

The idea of folding is similar to a two-steps ADC: both structures utilize two lower resolution quantizers to implement one higher resolution ADC. However, folding ADCs use analog preprocessing to generate "residue" at the same instant that the MSBs are produced from the coarse quantizer. The total resolution of the folding ADC is $N_B = n_{MSB}+n_{LSB}$, where n_{MSB} and n_{LSB} are the numbers of bits resolved in the coarse and fine quantizers, respectively.

We could consider , as example, that in a 5-bit folding ADC, a total of 10 (3 for coarse and 7 for fine quantizer) comparators are needed, while a 5-bit full-flash ADC needs 31 comparators. A folding ADC reuses comparators so that the total number of comparators can be reduced by a folding factor (F_F), here 4.

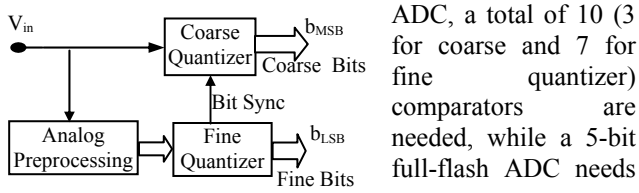


Fig. 1. Example of 5-bits folding ADC.

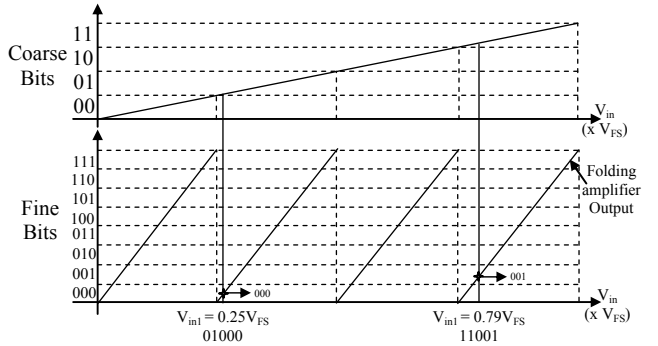


Fig. 2. Residue waveform at input of second-stage ADC.

In the folding architecture the analog preprocessing segments represent the most important part of the circuit because both the coarse and fine quantizer are full flash ADC. There are several methods to realize these circuits. The basic configuration is based on diodes [5], very simple to realize but it suffers when a large input swing is required. Another configuration is based on current-mirror that can be used to implement piecewise linear transfer characteristic of folding amplifier. The cascade current mirror version is strongly suitable for low voltage low power design, but the length of transistor have to be large if we want to obtain adequate accuracy, with disadvantage of low speed [6]. Another technique uses folding amplifier based on hyperbolic tangent transfer function of voltage differential pairs. This scheme solve bandwidth problem, but it suffers of intrinsic output current distortion that limits the number of folds [7]. Some of these drawbacks are overcome by wired-OR configuration at the differential pair outputs to reduce the common-mode output signal and to provide buffering, but this circuit still presents some problems due the threshold perturbing effects of a single-ended reference scheme [8].

A first approach that uses channels configuration is reported in [9] where each channel is divided in two parts: the first realizes the subtraction between the sampled input signal coming from the Track and Hold (T/H) and the reference voltage, while the second transfers the remaining analog voltage to the second ADC flash by means of electronic switches. Although this configuration is simple to realize the use of a summing node for each channel makes the power consumption high, moreover, the switches driving signal is the same that has to be transferred and this situation could create instability problem for high resolution.

3. THE CIRCUIT PROPOSED

The new architecture is composed by 2^n channels that realize the signal pre-processing (Fig. 3).

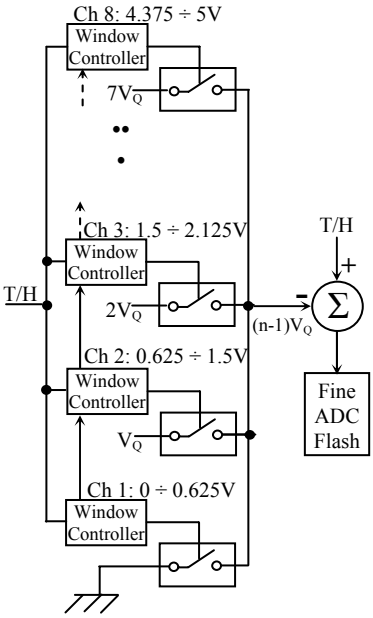


Fig. 3. Block scheme of the proposed circuit

Each channel is composed by a NMOS switch that, thanks to a pilot circuit (or window controller), is activated for prefixed range of input values. When the n^{th} switch is closed, the channel sends to the inverting input of a subtracter circuit a voltage equal to n-1 times the quantum voltage (V_Q). The outputs of the channels converge towards the subtracter that has, on the non-inverting pin, the input voltage (V_{in}). The difference between V_{in} and the increasing multiple of V_Q, that better rounds down the V_{in}, is the input of the fine quantizer and it is always included between 0 V and V_Q. The switch of the n^{th} channel has on the source a voltage equal to n-1 times the quantum; on the body there is a negative value able to maintain the body-drain p-n junction inversely polarized; the drain is connected with the subtracter, while the gate is driven by the control circuit. The latter has

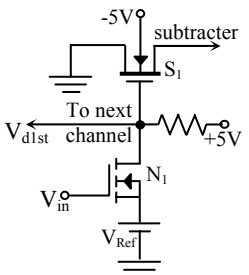


Fig. 4. First channel circuital scheme

to generate a signal that, for the whole input range, is high only for input included between n-1 and n times V_Q (considering the nth channel), and low otherwise, thus to keep the switch close only in this voltage range. In fact, a NMOS is in linear region only when the voltage difference between gate and source is higher than threshold voltage V_{TH}, while it is in cut-off region when V_{GS} is lower than V_{TH}. Using a ramp, that represents all input possible values, we analyze only the first channel (Fig. 4).

This has to give a voltage equal to zero for voltage input values between zero and V_Q. Its switch (S_1) has the source connected to ground. The gate signal has to be a +5 V value only when the ramp is lower than V_Q. To obtain this, we used another NMOS (N_1), as inverting circuit, with the input signal applied to its gate, with a constant voltage on its source, which allows fixing the commutation value from interdiction to linear region, and, at least, a resistor drain supplied by +5 V. The drain is then connected to the gate of S_1. In this way we realize the required functionality for the first channel as indicate in the following relations:

- $0 \le V_{in} < V_Q$: $N_1 \rightarrow$ OFF, $V_{d1st} \rightarrow$ +5 V, $S_1 \rightarrow$ ON;
- $V_{in} \ge V_Q$: $N_1 \rightarrow$ ON, $V_{d1st} \rightarrow V_{Ref}$, $S_1 \rightarrow$ OFF.

The next channels differ from first, only for the driving circuit (Fig. 5). Still considering a ramp as V_{in}, the driving signal has a low level, for V_{in} lower than $(n-1)V_Q$, an high level up to nV_Q and still low level for higher values. The circuit is realized by an NMOS (N_n) and a PMOS (P_n). The latter is polarized by two resistors between +5 V and -5 V;

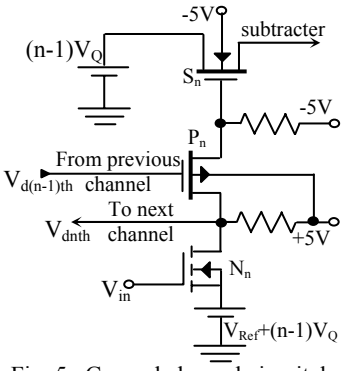


Fig. 5. General channel circuital scheme.

when the driving signal V_d, coming from the previous stage, has a +5 V value, P_n is OFF and consequently S_n is OFF; when V_d reaches $V_{Ref}+(n-1)V_Q$, P_n becomes ON like S_n. N_n results OFF until V_{in} overcomes the corresponding multiple of V_Q. This brings OFF P_n too and, consequently, S_n, as shown in simulation (Fig. 6).

- $V_{in} < (n-1)V_Q$: $V_{d(n-1)th} \rightarrow$ +5 V, $N_n \rightarrow$ OFF, $P_n \rightarrow$ OFF, $V_{dnth} \rightarrow$ +5 V, $S_n \rightarrow$ OFF;

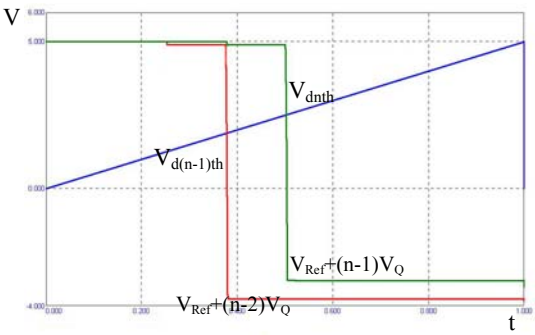


Fig. 6. Driving circuit commands.

- $(n-1)V_Q \le V_{in} < nV_Q$: $N_n \rightarrow$ OFF, $V_{d(n-1)th} \rightarrow V_{Ref}+(n-1)V_Q$, $P_n \rightarrow$ ON, $V_{dnth} \rightarrow$ +5 V, $S_n \rightarrow$ ON;
- $V_{in} \ge nV_Q$: $N_n \rightarrow$ ON, $V_{d(n-1)th} \rightarrow V_{Ref}+(n-1)V_Q$, $V_{dnth} \rightarrow V_{Ref}+nV_Q$, $P_n \rightarrow$ OFF, $S_n \rightarrow$ OFF;

The V_d driving signal, coming from the n-1th channel, drives the nth channel creating a cascade connection between successive channels.

The last channel has a driving circuit similar to the first, that is a NMOS which source is hold to a $V_{Ref}+(n-1)V_Q$ voltage and driven on gate by V_d coming from the previous channel (Fig. 7).

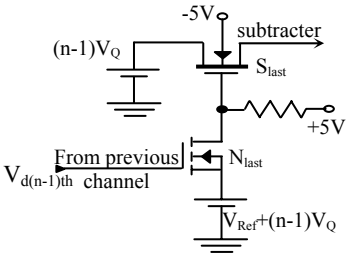


Fig. 7. Final channel circuital scheme.

- $V_{in} < (n-1)V_Q$: $V_{d(n-1)th} \rightarrow$ +5 V, $N_{last} \rightarrow$ OFF, $S_{last} \rightarrow$ OFF;
- $V_{in} \ge (n-1)V_Q$: $V_{d(n-1)th} \rightarrow V_{Ref}+(n-1)V_Q$, $N_{last} \rightarrow$ ON, $S_{last} \rightarrow$ ON;

Connecting all channels outputs, we obtain a "staircase" that grows with steps of V_Q. This, sent to the subtracter together with V_{in}, produces the desired signal in coincidence to the wanted intervals, that is values always included between 0 V and V_Q (simulation shown in Fig. 8). The fine quantizer will convert this signal.

The simulations of the circuit are obtained from MicroCap 7.0.

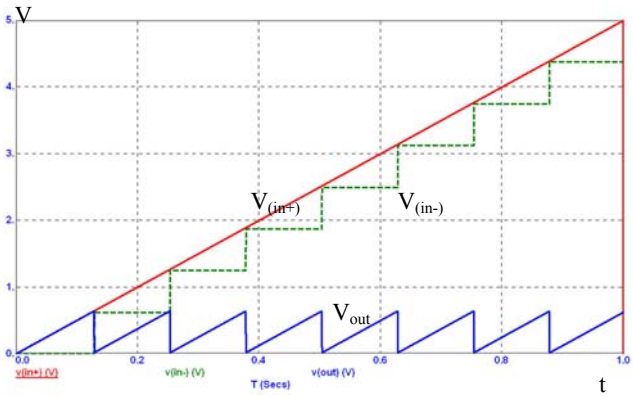


Fig. 8. Inputs and Output simulation of final subtracter: v(in+): input Voltage non inverting input of the subtracter; v(in-): "staircase" inverting input of the subtracter; v(out): output of the subtracter.

4. THE EXPERIMENTAL RESULTS

The circuit has been realized with discrete components. For the NMOS switch, we used the Calogic enhancement NMOS transistor IT1750 that has the body separated by the source, with values for $V_{GS(th)}$ included between 0.5 and 3 V, a $r_{DS(ON)}$ of 50 Ω and an I_{DSS} of 10 nA. For the PMOS we used 3N163 always of Calogic, with a $V_{GS(th)}$ included between 2 and 5 V, a typical $r_{DS(ON)}$ of 250 Ω and an I_{SDS} of typically 400 pA.

Fig. 9 shows the schematic. It's easy to appreciate the simplicity of implementation of each channel and the unique final summing node that warrants low consumption.

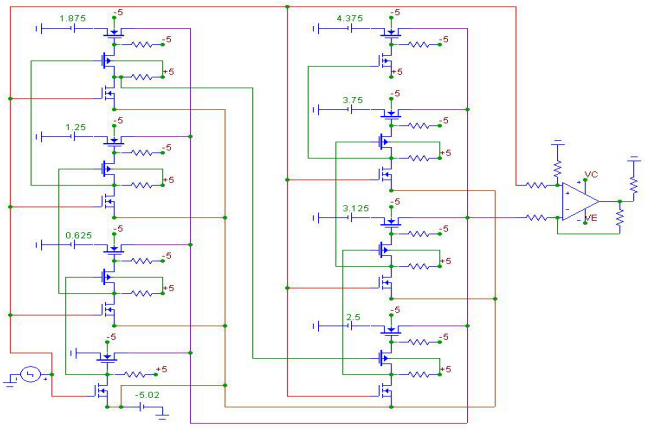
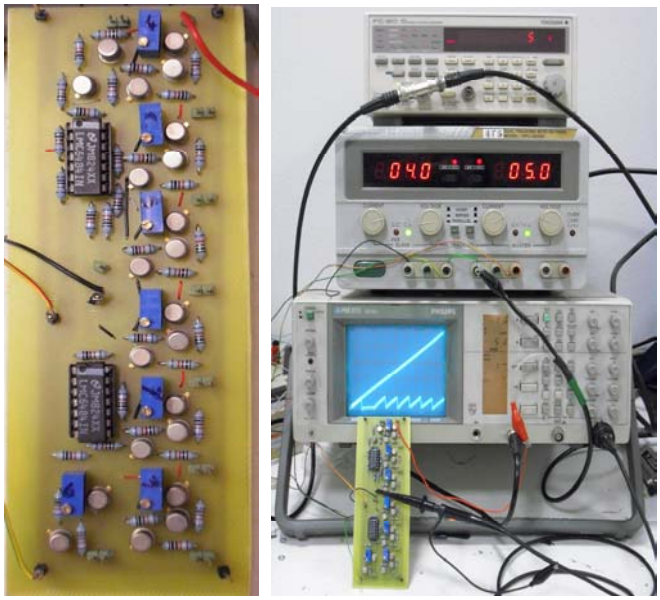


Fig. 9. Schematic of the circuit.

Fig. 10a shows the realized circuit, while the Fig. 10b shows the measurement bench with a stabilized energy supplier, a Philips PM3070 oscilloscope and a Yokogawa FG120 function generator.



a b

Fig. 10. Discrete PCB circuit (a) and Measurement Bench (b).

Fig. 11 shows the oscilloscope output circuit signal when the input is a ramp function between 0 and 5 V.

Fig. 10b and the Fig. 11 show as the circuit realizes the pure linear folding transfer function. On the oscilloscope, it is possible to read a voltage quantum of 626 mV because its resolution is 2 mV. The maximum resolution obtainable by this circuit with the Calogic's components is 78.125 mV equal to a possible discrete pure linear analog preprocessing folding of 64 channels.

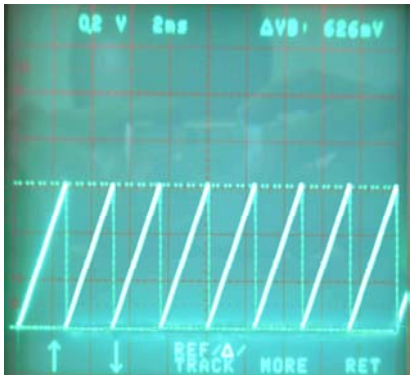


Fig. 11. Oscilloscope test

5. CONCLUSION

Talking of conclusions is too early for this work that is still "in itinere" anyway we surely described a new kind of analog preprocessing circuit for linear folding ADC.

We underline the simplicity of the scheme. For the first channel and for the last only two mosfets are used, while, for the other channels, three. A simple resistor divider, connected to the sources of the NMOS switches, gives the quantum voltage multiplies. The consumption of this apparatus is very low, implementing, besides the channels, only an operational amplifier for the subtracter. The circuit, after a wide simulation, has been realized by discrete components and tested.

The next step will be to realize an integrated circuit of the proposed A/D to evaluate some characteristics as bandwidth or typical conversion errors, specific for this architecture, and to improve the resolution of this structure.

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