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FAULT DIAGNOSIS OF FULLY DIFFERENTIAL CIRCUITS IN ELECTRONIC EMBEDDED SYSTEMS

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Abstract – A new Built-In-Self-Test scheme for diagnosis of analog fully differential circuits in embedded mixed-signal microsystems is presented. The measurement procedure is realized by the internal resources of the microcontroller. The real and imaginary parts of the output differential voltage are measured with common-mode excitation of the circuit under test (CUT). The diagnosis procedure is based on the fault dictionary stored in the memory of the microcontroller. The dictionary is created in polar coordinates during the design of the system.

Keywords BIST, fault diagnosis, fully differential circuits

1. INTRODUCTION

Built-In-Self-Test (BIST) technique is very attractive to overcome the problems of testing embedded analog blocks to which external accessibility through the primary I/O is limited. They reduce the need of external testing by moving ATE functions to the chip or board. Usually the BIST technique provides go/no-go testing. In the paper we consider a BIST scheme with functionality extended to fault diagnosis.

The architecture of the circuit under test (CUT) is fully differential. Such a solution has been very popular in the design of filters, A/D converters etc. because of many advantages. Due to the inherent redundancy within the circuit structure, fully differential circuits are also easily testable.

In [1] a fault-oriented testing method for fully differential circuits which employs the common-mode excitation of the CUT is proposed. It is shown that the method is superior in test quality over the previously reported one that exploits a differential-mode excitation.

In order to extend the method to fault localization we use a pattern-matching approach which is known as the “fault dictionary”.

2. FAULT DICTIONARY APPROACH

The fault-dictionary approach first determines the CUT responses that are likely to occur, given the anticipated faults. The simulated circuit responses make up the fault dictionary. During testing, the measurement data are compared against the responses from the fault dictionary and the data that best match the test circuit’s measurement data, determine the faulty component.

2.1. Testing with the common-mode excitation

As an example of testing with the common-mode excitation, let us consider the fully differential Deliyannis-Friend band-pass filter shown in Fig. 1.

Fault detection is performed by applying excitation at the reference input of the output common-mode voltage and with both inputs grounded, as shown in Fig.1. It has been shown in [1] that such test architecture gives result equivalent to testing the transfer function G_{DC}. This function relates the output differential voltage to the input common-mode voltage [2]. The measured output differential voltage is theoretically zero in the case of a fault-free (symmetrical) circuit under test and become non-zero if the symmetry is violated by a faulty component.

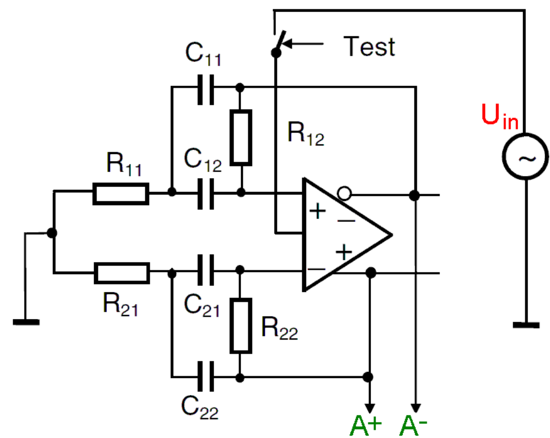

Fig. 1. Example of the tested analog part – fully differential implementation of the band-pass Deliyannis-Friend filter

The nominal values for R11, R12, R21, R22 are [1130 Ω, 4480 Ω, 1130Ω, 4480 Ω], respectively, all the capacitors have the same value C11-C22 = 0,1 μF. The filter was realized on the basis of the Texas Instruments THS 4131 op-amp.

Several factors have contributed to making analog circuits fault diagnosis a technical challenge, first of all the problem of tolerance. Due to manufacturing tolerances, the responses of the CUT show statistical distribution and a residual differential voltage is generated even when no faults

occur. It is necessary to apply a detection threshold to differentiate between faulty and fault-free responses, selected properly with the aid of tolerance analysis.

2.2. Estimation of manufacturing process-induced defect level

In [3] a probabilistic model of performances of the CUT has been derived. The probability distribution function (pdf) of magnitude *z* of the residual voltage has the form:

$$f_Z(z)=\frac{z}{\sigma_X\sigma_Y\sqrt{1-r^2}}e^{-\frac{z^2}{2(1-r^2)}a}\; I_0\left(\frac{z^2}{2(1-r^2)}\sqrt{b^2+c^2}\right) \quad (1)$$

where *x*, *y* are the real and imaginary parts of the residual voltage, σ_X, σ_Y are the respective standard deviations, *r* is the correlation coefficient between *x* and *y*, $a=\frac{\sigma_X^2+\sigma_Y^2}{2\sigma_X^2\sigma_Y^2}$, $b=\frac{\sigma_X^2-\sigma_Y^2}{2\sigma_X^2\sigma_Y^2}$, $c=\frac{r}{\sigma_X\sigma_Y}$,
I_0 – the modified Bessel function of the first kind and zero-th order.

The parameters of distribution (1): σ_X, σ_Y, r can be evaluated performing the expansion of the network function of interest using Taylor series expansion around the point that represents the mean values of components and truncating the Taylor series after the first partial derivatives [1]. For example, assuming 1% component tolerances with uniform distribution and frequency of testing signal equivalent to the center of the frequency response of the filter, we obtain: $\sigma_x = 8.55$ mV, $\sigma_Y = 10.77$ mV and r = 0.

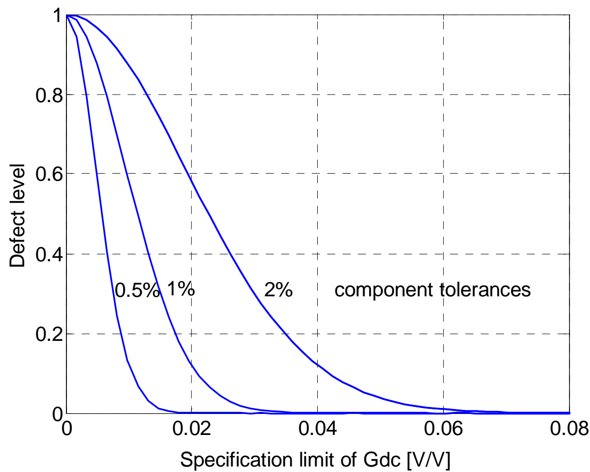

Fig. 2. The manufacturing process induced defect level versus specification limit of G_{DC} and component tolerances

The pdf (1) was applied for estimation of the manufacturing process induced defect level (1-yield), i.e., the likelihood of the CUT exceeding a given specification limit due to manufacturing tolerances. An approach to estimate the probability of a specification violation is to integrate the tail of pdf (1) outside the specification limit of G_{DC} as follows:

$$1-Y(G_{DCspec})=\int_{G_{DCspec}}^{+\infty} f_Z(z)dz \quad (2)$$

The plots of calculated tail probability due to component tolerances from the range of 0,5% - 2%, versus specification limits of $G_{DC,}$ are presented in Fig. 2. For tight specification limit, the number of circuits failing to meet this limit is high, resulting in a low yield. For wider specification limit, the number of failing circuits decreases, which results in higher yield but the less competitive the product in the market. For specification limit G_{DCspec} = 0.044 V/V the integral (2) evaluates to 1-Y(G_{DCspec}) = 77 ppm.

2.3. Determination of the value of the fault detection threshold U_{A_th}.

We need to find the fault detection threshold to separate the faulty circuits from the fault-free ones. The CUT test is subject to measurement uncertainty that causes the risk of taking the wrong decision, which results in higher defect level. The test related defect level, is the probability of passing a defective device to the customer. In order to guarantee low test related defect level, the guard-band that needs to account the variation of the measurement result induced by noise, must be applied during the fault detection threshold U_{A_th} determination. Tightening the fault detection threshold will lead to lower the defect level but also to higher the test yield loss (Fig. 3). The data for analysis was obtained from a probability framework for evaluation of test quality metrix presented in [1], which is based on the probabilistic model of performances of the CUT (1) and a probabilistic model for measurement process proposed by Rossi [4]. Many authors suggest that the low defect level is more important than the low yield loss because it is at least ten times more expensive to ship a bed circuit than to discard a good one.

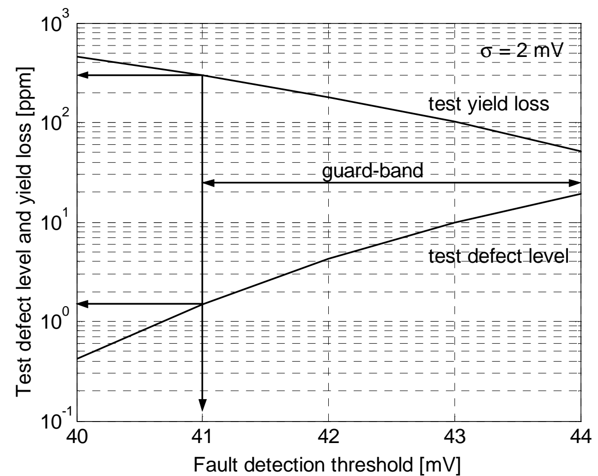

Fig. 3. Test defect level and yield loss versus the setting of the fault detection threshold (for the standard deviation of measurements σ =2 mV)

For 1 V amplitude of the testing signal and the assumed standard deviation of measurements σ =2 mV, the fault

detection threshold U_{A_th} should be set at 41 mV, to obtain at least 3 mV guard band. This guard-band reduces the test related defect level to 2 – 3 ppm, and increases the test yield loss to 300 ppm.

2.3. The fault dictionary

The fault dictionary has the form of a family of identification curves in polar coordinates generated by carrying out a Monte Carlo simulation on a PC. With regard to the limited size of the memory, the fault dictionary should have the smallest possible size. For the assumed range of variability from $0.1 \cdot x_{i\,nom}$ to $10 \cdot x_{i\,nom}$,($x_{i\,nom}$ – the nominal value of the i-th component), the values of components are chosen using the log space function. Finally the fault dictionary is converted into the file with the full code of a program, compiled to a HEX file and placed in the program memory of the microcontroller in the ISP mode.

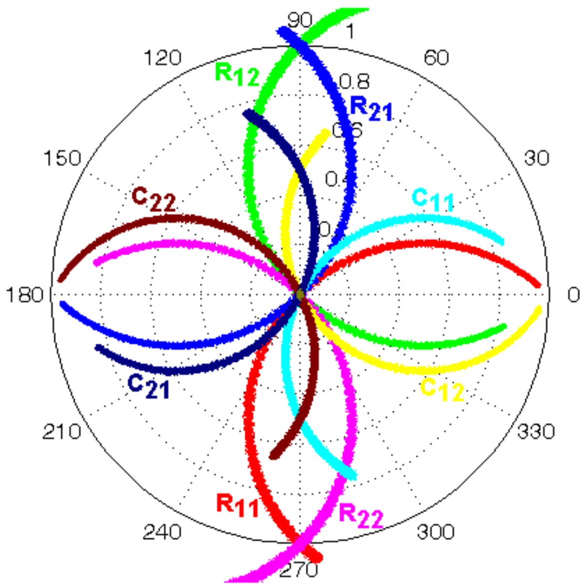

Fig. 4. Localization belts of the tested analog part (Fig. 1) for 1% component tolerances

The fault dictionary contains descriptions of all I localization belts shown in Fig. 4. From Fig. 4 it is seen that in the polar coordinates each i-th belt has the shape of a semicircle. Hence, it can be described by the magnitude A_i and the phase ϕ_i fulfilling (3)

$$z = A_i \cdot sin(\phi - \phi_i) \tag{3}$$

where (z,ϕ) are coordinates of the point in the polar coordinate system.

The values ϕ_i and A_i are determined from two points (ϕ_{i1}, A_{i1}) and (ϕ_{i2}, A_{i2}) generated for two values of the i-th component during simulation of the tested analog circuit.

Basing on (3) and these points we can write the following relationships:

$$\begin{cases} A_{i1} = A_i \cdot \sin(\phi_{i1} - \phi_i) \\ A_{i2} = A_i \cdot \sin(\phi_{i2} - \phi_i) \end{cases} \tag{4}$$

Eq. (4) can be write out to the form:

$$\begin{cases} A_{i1} = \sin(\phi_{i1}) \cdot A_i \cdot \cos(\phi_i) - \cos(\phi_{i1}) \cdot A_i \cdot \sin(\phi_i) \\ A_{i2} = \sin(\phi_{i2}) \cdot A_i \cdot \cos(\phi_i) - \cos(\phi_{i2}) \cdot A_i \cdot \sin(\phi_i) \end{cases} \tag{5}$$

Setting

$$v_i = A_i \cdot \cos(\phi_i),\ w_i = A_i \cdot \sin(\phi_i) \tag{6}$$

the relationships (5) can be transformed to the form:

$$\begin{cases} A_{i1} = \sin(\phi_{i1}) \cdot v_i - \cos(\phi_{i1}) \cdot w_i \\ A_{i2} = \sin(\phi_{i2}) \cdot v_i - \cos(\phi_{i2}) \cdot w_i \end{cases} \tag{7}$$

After transformations we obtain the following equations for values of v_i and w_i:

$$v_i = \frac{A_{i1} \cdot \cos(\phi_{i2}) - A_{i2} \cdot \cos(\phi_{i1})}{\sin(\phi_{i1}) \cdot \cos(\phi_{i2}) - \cos(\phi_{i1}) \cdot \sin(\phi_{i2})} \tag{8a}$$

$$w_i = \frac{A_{i2} \cdot \sin(\phi_{i1}) - A_{i1} \cdot \sin(\phi_{i2})}{\sin(\phi_{i1}) \cdot \cos(\phi_{i2}) - \cos(\phi_{i1}) \cdot \sin(\phi_{i2})} \tag{8b}$$

Setting

$$A_i = \frac{v_i}{\cos(\phi_i)},\ \phi_i = \arctan\left(\frac{w_i}{v_i}\right) \tag{9}$$

we obtain the formulae for the magnitude A_i and the phase ϕ_i describing the i-th belt:

$$A_i = \frac{A_{i2} \cdot \sin(\phi_{i1}) - A_{i1} \cdot \sin(\phi_{i2})}{\cos(\phi_i) \cdot (\sin(\phi_{i1}) \cdot \cos(\phi_{i2}) - \cos(\phi_{i1}) \cdot \sin(\phi_{i2}))} \tag{10a}$$

$$\phi_i = \arctan\left(\frac{A_{i2} \cdot \sin(\phi_{i1}) - A_{i1} \cdot \sin(\phi_{i2})}{A_{i1} \cdot \cos(\phi_{i2}) - A_{i2} \cdot \cos(\phi_{i1})}\right) \tag{10b}$$

The magnitude A_i and the phase ϕ_i can be represented by values v_i and w_i (see (9)). Thus basing on this fact we eliminated expressions with the angle ϕ_i from the localization condition which considerably simplifies calculations executed during the self-testing process. Hence, v_i, w_i are indirect parameters describing the i-th localization belt.

The third parameter η_i describes the average width of the i-th belt. A value of the parameter η_i depends on tolerance values of no-faulty circuit components. E.g. if values of the component tolerance increase, the widths of all belts also increase. Hence, the following algorithm of the η_i coefficient determination is proposed:

- In the first step of the algorithm M points with coordinates (v_i^m, w_i^m) $m = 1, .., M$ representing two end areas of the i-th localization belt in the indirect parameters space are generated using the Monte Carlo method. The first end area $\{(v_{i,0.1}{}^m, w_{i,0.1}{}^m)\}_{m=1,..,M}$ is generated for the $0.1 \cdot x_{i\,nom}$ value of the i-th component, the second one $\{(v_{i,0.1}{}^m, w_{i,0.1}{}^m)\}_{m=1,..,M}$ for the $10 \cdot x_{i\,nom}$ component value.
- Next, for these areas the following parameters are defined and determined:

$$\eta_i^{0.1} = \max\left\{ \left| \max_{m=1,\ldots,M} \{v_{i,0.1}^m\} - \min_{m=1,\ldots,M} \{v_{i,0.1}^m\} \right|, \right. \quad (11a)$$

$$\left. \left| \max_{m=1,\ldots,M} \{w_{i,0.1}^m\} - \min_{m=1,\ldots,M} \{w_{i,0.1}^m\} \right| \right\}$$

$$\eta_i^{10} = \max\left\{ \left| \max_{m=1,\ldots,M} \{v_{i,10}^m\} - \min_{m=1,\ldots,M} \{v_{i,10}^m\} \right|, \right. \quad (11b)$$

$$\left. \left| \max_{m=1,\ldots,M} \{w_{i,10}^m\} - \min_{m=1,\ldots,M} \{w_{,10i}^m\} \right| \right\}$$

– Finally, we chose the maximum value which will be represented the width of the i-th belt:

$$\eta_i = \max\{\eta_i^{0.1}, \eta_i^{10}\} \quad (12)$$

Hence, the full fault dictionary has the following very compressive form $\{U_{A_th}, \{ v_i, w_i, \eta_i\}_{i=1,\ldots,I}\}$.

The localization part of the fault dictionary for the circuit from Fig. 1 is presented in Table 1. The detection part consists of only one element $U_{A_th} = 8$ [×5 mV].

Table 1. The fault dictionary for the circuit from Fig. 1.

Faulty component	v_i [×5 mV]	w_i [×5 mV]	η_i [×5 mV]
R11	-200	200	6
R12	202	200	6
R21	200	-200	6
R22	-202	-200	6
C12	100	200	4
C11	-100	200	4
C22	-100	-200	6
C21	100	-200	4

The parameters U_{A_th}, v_i, w_i, η_i, are converted to the form compatible with the direct measurement result form of the microcontroller ADC with the internal voltage reference V_{Ref} = 2.56 V. Hence, the microcontroller operates on integer values, and what it is worth to underline, the ADC results are directly used by diagnosis procedures, what simplifies calculations made during the fault detection and localization.

3. SELF-TESTING OF THE ANALOG PART

The self-testing procedure of the analog part of the system is run by the control unit (represented by the microcontroller). The control unit together with its internal measurement devices (ADCs, timers) creates the reconfigurable BIST [5, 6]. It consists of two stages: the measurement procedure using the internal ADC triggered by the internal timer of the microcontroller to measure the magnitude and the phase of the differential output voltage of the analog part, and the fault detection and localization procedure, where the microcontroller, based on the fault dictionary and the measurement results, carries out fault detection, and when a fault is detected, its localization.

3.1. The measurement procedure

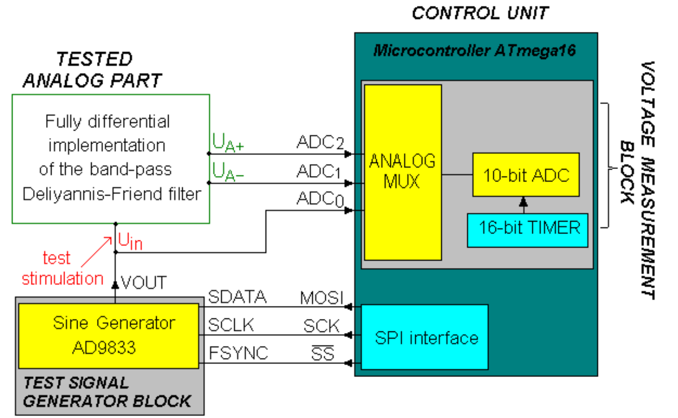

Fig. 5. Example of the electronic embedded system in the self-testing mode of the analog part

Fig. 5 shows the electronic embedded system working in the self testing mode of the analog part. The analog part is stimulated by a programmable sinusoidal generator. The input signal u_{in} is sampled by the ADC in moments established by the 16-bit Timer 1 of the microcontroller [7] similarly as in [8]. In the same way the output differential signal u_A is also sampled (Fig. 6). But, in this case the ADC works in the Differential Gain Channels (DGC) mode. Hardware possibility of sampling of differential signals by the ADC significantly simplifies the BIST structure and the measurement algorithm, what is an advantage of this solution.

It is seen from Fig. 6, that each signal is sampled three times, where time distances between samples are set to one fourth of the period T. Time distances between samples for subsequent signals are equal to a half of the period. We can say that it allows to sample all signals at the same moments in relation to beginning of sampling, because sampling of the next signal is shifted by a period. Sampling of the input signal u_{in} is needed to establish a random shift time T_α of the sampling series. The third sample of each signal is used for elimination of the voltage offset. The first and second samples of the output differential signal u_A are used to calculate its real x_A and imaginary y_A parts and its magnitude U_A.

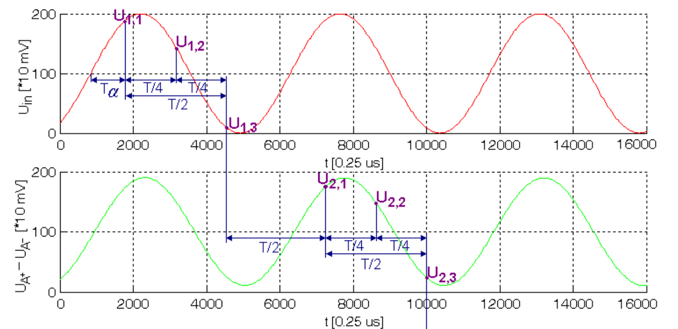

Fig. 6. Timings of the measured signals during the self-testing procedure

The idea of the measurement procedure is as follows. We know the values of the amplitude U_1 and the period T of the stimulant signal u_{in}. We measure voltage samples $u_{1,1}$, $u_{1,2}$, $u_{1,3}$ of the u_{in} signal and voltage samples $u_{2,1}$, $u_{2,2}$, $u_{2,3}$ of the u_A output signal in the way shown in Fig. 6.

Next, we calculate and eliminate from all samples the offset $u_{n,offset}$:

$$u_{n,offset} = \frac{u_{n,1} + u_{n,3}}{2}, \; n = 1, 2 \tag{13}$$

We start to sample the sinusoidal signal in a random moment moving in relation to beginning of this signal about a random shift time T_α as shown in Fig. 6. Thus we have to eliminate this unknown time, that is we calculate a correction following from the time T_α expressed as sine and cosine of the angle $\alpha = \frac{2\pi}{T} T_\alpha$:

$$\sin\alpha = \frac{u_{1,1}}{U_1} \qquad \cos\alpha = \frac{u_{1,2}}{U_1} \tag{14}$$

We assume that the output differential signal u_A has the form $u_A = x_A + jy_A$. The voltage samples are described by the equations:

$$\begin{cases} u_{2,1} = U_A \sin(\alpha + \phi_A) \\ u_{2,2} = U_A \sin(\alpha + \phi_A + \frac{\pi}{2}) \end{cases} \tag{15}$$

where ϕ_A is the phase of the output differential signal.

Eq. (15) can be write out to the form:

$$\begin{cases} u_{2,1} = U_A \cdot \sin(\alpha) \cdot \cos(\phi_A) + U_A \cdot \cos(\alpha) \cdot \sin(\phi_A) \\ u_{2,2} = U_A \cdot \cos(\alpha) \cdot \cos(\phi_A) - U_A \cdot \sin(\alpha) \cdot \sin(\phi_A) \end{cases} \tag{16}$$

Setting $\quad x_A = U_A \cdot \cos(\phi_A), \; y_A = U_A \cdot \sin(\phi_A) \quad (17)$

and putting them to (16) we obtain the equations:

$$\begin{cases} u_{2,1} = x_A \cdot \sin(\alpha) + y_A \cdot \cos(\alpha) \\ u_{2,2} = x_A \cdot \cos(\alpha) - y_A \cdot \sin(\alpha) \end{cases} \tag{18}$$

Determining x_A and y_A we obtain:

$$\begin{cases} x_A = u_{2,1} \cdot \sin(\alpha) + u_{2,2} \cdot \cos(\alpha) \\ y_A = u_{2,1} \cdot \cos(\alpha) - u_{2,2} \cdot \sin(\alpha) \end{cases} \tag{19}$$

Next, we put (14) to (19), what after transformations gives the following relationships:

$$\begin{cases} x_A = (u_{2,1} \cdot u_{1,1} + u_{2,2} \cdot u_{1,2}) \cdot \left(\frac{1}{U_1}\right) \\ y_A = (u_{2,1} \cdot u_{1,2} - u_{2,2} \cdot u_{1,1}) \cdot \left(\frac{1}{U_1}\right) \end{cases} \tag{20}$$

Because U_1 is constant and known, also the parameter $\xi = 1/U_1$ is constant and known, what considerably simplifies calculations of the values x_A and y_A. It follows from the fact, that calculations base only on addition, subtraction and multiplication operators.

Thus, we obtain the following formulae on the real x_A and imaginary y_A parts and the magnitude U_A and its square U_{A_square} of the output differential signal:

$$\begin{cases} x_A = (u_{2,1} \cdot u_{1,1} + u_{2,2} \cdot u_{1,2}) \cdot \xi \\ y_A = (u_{2,1} \cdot u_{1,2} - u_{2,2} \cdot u_{1,1}) \cdot \xi \\ U_{A_square} = x_A \cdot x_A + y_A \cdot y_A \\ U_A = \sqrt{U_{A_square}} \end{cases} \tag{21}$$

Hence, the microcontroller proceeding according to the measurement procedure whose algorithm is shown in Fig. 7, measures three voltage samples of the stimulus and the output differential signal, and next calculates all parameters of the output differential signal based on (21).

The algorithm of the measurement procedure consists of two parts (Fig. 7). The first part is responsible for control of the measurement. The main function starts the timer and waits for the end of sampling, that is it waits for measurement of six voltage samples. The interrupt service of the timer starts the ADC conversion and actualizes the counting time between next samples. The interrupt service of the ADC conversion complete saves the voltage samples and changes the channel of the analog multiplexer. The calculation part computes the magnitude, its square and the real and imaginary parts of the output differential signal according to (21).

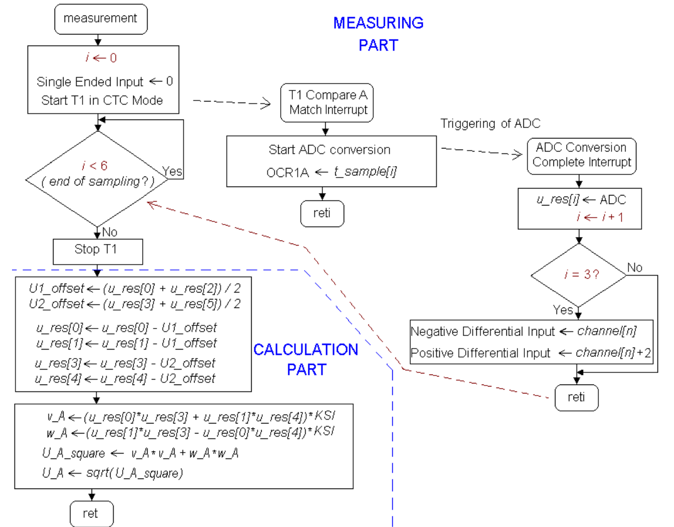

Fig. 7. The algorithm of the measurement procedure

3.2. Fault diagnosis procedure

The fault diagnosis procedure consists of two steps: fault detection and fault localization.

The fault *detection* is very simple and it bases on the test if the measured magnitude of the output differential signal U_A is smaller than the value of the threshold U_{A_th}.

Thus, if the condition $U_A \le U_{A_th}$ is fulfilled the detection function returns 0, what means that the tested fault circuit is fault free (Listing. 1). Else it returns the MAX value, what calls the localization functions.

```
uint8_t detection(void)
{
if(U_A < U_th) return(0);
else return(MAX);
}
```

Listing 1. The code of the detection function

In the *localization* step for all I components the localization condition is tested. Generally this condition has the form:

$$\left|U_A - A_i \cdot \sin(\phi_A - \phi_i)\right| \le \eta_i \quad (22)$$

which can be write out to the form:

$$\left|U_A - A_i \cdot \cos(\phi_i) \cdot \sin(\phi_A) - A_i \cdot \sin(\phi_i) \cdot \cos(\phi_A)\right| \le \eta_i \quad (23)$$

because of (6), the (23) can be presented in the form:

$$\left|U_A - \nu_i \cdot \sin(\phi_A) - w_i \cdot \cos(\phi_A)\right| \le \eta_i \quad (24)$$

To eliminate the expression with the phase ϕ_i, we multiply the inequality (24) by the magnitude U_A:

$$\left|U_{A_square} - \nu_i \cdot U_A \cdot \sin(\phi_A) + w_i \cdot U_A \cdot \cos(\phi_A)\right| \le \eta_i \cdot U_A \quad (25)$$

Putting (17) to (25) we obtain the final localization condition:

$$\left|U_{A_square} - \nu_i \cdot y_A + w_i \cdot x_A\right| \le \eta_i \cdot U_A \quad (26)$$

where: ν_i, w_i, η_i – values describing the i-th localization belt.

The localization function (Listing 2) calculates and tests the localization condition (26) for all I elements, and if for given i-th element this condition is fulfilled, it sets the i-th bit in the `fault_i` variable.

```
uint8_t localization(void)
{
uint8_t i, fault_i;
int16_t left, right;

fault_i = MAX;

for(i=0; i<I; i++)
  {
  left = U_A_square - (v_i[i]*y_A) + (w_i[i]*x_A);
  right = ni_i[i]*U_A;

  if(left < right)
    {
    fault_i |= (0x01 <<i);
    }
  }
return(fault_i);
}
```

Listing 2. The code of the localization function

The control unit according to the fault diagnosis result, obtained by the detection and localization procedures, can run a definite alarm and it can send the results via any wired or wireless interface to the main computer.

One should underline the fact that these self-testing procedures of analog parts of the electronic embedded systems should be treated as part of full self-testing of this system, where the software, memories, the microprocessor core, digital circuits and remaining important components of the system are tested. Hence, self-testing procedures of analog circuits and the fault dictionary were elaborated with regard to minimal occupation of the program memory space of the control unit and minimal requirement on computing power.

4. CONCLUSIONS

In the paper, the BIST scheme for a fully differential analog part of an electronic embedded system covering circuit measurement and fault diagnosis is presented. The diagnosis procedure consists of two steps. In the first step the self-test (fault detection) is performed. In the second part fault localization is made.

The localization belts in the polar coordinate system have the shape of a semicircle, crossing the origin. Each belt can be represented by only three parameters. Hence, the fault dictionary has a very concise form.

To minimize the probability of an incorrect test decision in the first step due to manufacturing tolerances and measurement uncertainty, the fault detection threshold has been thoroughly chosen by analysis with the aid of a probabilistic model of the CUT performances.

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