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ON THE DESIGN OF LOW-POWER SIGNAL CONDITIONERS FOR RESISTIVE SENSORS

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Abstract – This work analyzes power consumption in signal conditioning circuits for resistive sensors. We show that, for a given dynamic range for the measurand, simple conditioners based on voltage dividers or Wheatstone bridges directly connected to an analog-to-digital converter (ADC) do not usually have minimal power consumption. We develop analytical guidelines to achieve the optimal power design for signal conditioners and apply them to the actual design of the conditioner for an RTD sensor. We show that by adding a low-power amplifier plus a passive low-pass filter to a voltage divider sensor interface, the power consumption can be significantly reduced as compared to that of standard voltage dividers designed for maximal sensitivity.

Keywords: optimal power design, signal conditioning circuits, resistive sensors

1. INTRODUCTION

Power consumption has lately become a main issue in digital [1] and analog [2] electronic circuit design. Low-power design, traditionally associated to autonomous portable equipment [3], has gained momentum with the development of sensor networks and distributed data acquisition systems [4]. These two last areas in particular need low-power analog signal conditioning circuits but research efforts to reduce power consumption in these applications have mainly addressed communication protocols [5] without considering that many autonomous systems spend far more time (and energy) in measuring than in communicating. On the other hand, low-power analog design has traditionally focused more on reducing power consumption in each individual IC than on the optimal power design of the whole signal chain. Furthermore, to the best of our knowledge, power analysis or low-power design criteria are not usually considered for the most common sensor signal conditioners such as voltage dividers or Wheatstone bridges [6, 7, 8]. Rather, the trade-off between high sensitivity and linearity is addressed.

In this work we analyze power consumption in the measurement chain for resistive sensors. First, we establish the design guidelines that yield minimal power dissipation for a given dynamic range of the measurand. Then, we compare power dissipation in two designs for an RTD conditioner: one according to common practice and the other one according to the guidelines developed, and experimentally assess the benefits of the novel design approach proposed.

2. THEORETICAL ANALYSIS

Fig. 1 shows the basic measurement chain to convert a measurand into a digital value. We divide the analog signal conditioning block into the *interface circuit*, defined as the minimal circuitry to convert the sensor quantity into a voltage, and the *analog processor*, defined as the additional circuitry to match levels (e.g. gain/offset stages), reduce noise (e.g. filtering stages), demodulate, linearize, or any other analog signal processing function previous to the ADC [9].

Any measurement of a quantity x has a desired range x_{FS} ($= x_{max} - x_{min}$) and resolution Δx, whose quotient determines the so-called dynamic range [9] that should be ensured by each block of the measurement chain:

$$DR = \frac{x_{FS}}{\Delta x} \tag{1}$$

On the other hand, the total power consumption P_T of the measuring system is the sum of the power dissipated in each block,

$$P_T = P_s + P_i + P_a + P_{ADC} \tag{2}$$

being P_s, P_i, P_a, and P_{ADC} the power consumption of sensor, interface circuit, analog processor and ADC respectively.

The best design from the point of view of power dissipation is achieved when P_T is minimal for the dynamic range required for the application in hand. Because the sensor interface circuit depends on the particular sensor type

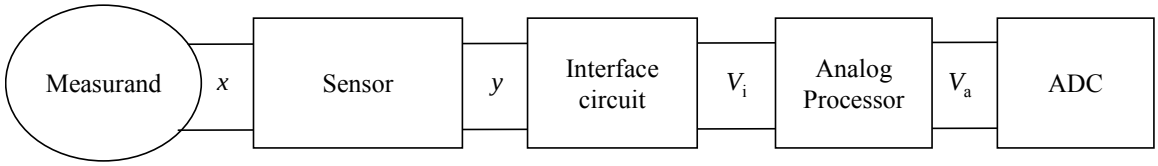

Fig. 1. Measurement chain to obtain a digital value from a measurand.

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we will address resistive sensors, which dissipate more power than, say, capacitive or self-generating sensors, and are more common than inductive sensors. In the following sections we will develop design guidelines by analyzing the power dissipation for signal conditioning stages in Fig. 1.

2.1. Resistive sensors and their interface circuits.

Resistive sensors are usually driven by a constant (reference) voltage source. Then, the highest available nominal resistance for the sensor type used will yield the lowest power consumption. For a constant current supply, the opposite would be true.

The commonest electronic interfaces for resistive sensors driven by a constant voltage are voltage dividers and Wheatstone bridges. Voltage dividers have lower power consumption than Wheatstone bridges and should therefore be preferred. The main shortcoming of voltage dividers is their larger output offset voltage, but this can be addressed at the system level by a convenient selection of the power supply rails and signal ground, by shifting voltage levels later in the signal chain, or by selecting an ADC with a resolution larger than that required to obtain the desired DR.

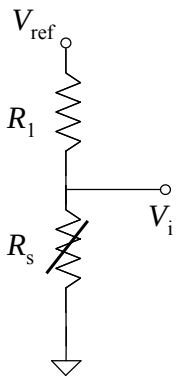

Fig. 2. Voltage divider interface for a resistive sensor R_s.

Fig. 2 shows a resistive sensor R_s in a voltage divider circuit. The power dissipated is:

$$P_s + P_i = \frac{V_{ref}^2}{R_1 + R_s} \tag{3}$$

where V_{ref} is the voltage supply and R_1 is the additional resistor. From (3), for a given sensor R_s, power dissipation can be reduced by increasing R_1 or by reducing V_{ref}.

The output voltage range is:

$$V_{i_{FS}} = V_{ref}\left(\frac{R_{s,max}}{R_1 + R_{s,max}} - \frac{R_{s,min}}{R_1 + R_{s,min}}\right) \tag{4}$$

where $R_{s,max}$ and $R_{s,min}$ are the maximum and minimum values of the sensor for the corresponding values of the measurand. It turns out that reducing $P_s + P_i$ by increasing R_1 or reducing V_{ref} implies a reduced output voltage range, hence a smaller dynamic range. This trade-off between power consumption and output voltage range can be overcome by adding gain blocks, but these will also dissipate power.

To avoid the use of extra blocks, in order to achieve a minimal system that has the desired dynamic range, a first design approach is to calculate R_1 to achieve the maximal output voltage range, hence the maximal dynamic range for a given resolution in the ensuing voltage measurement. For given V_{ref} and R_s, the R_1 value that maximizes the output voltage range is:

$$R_1 = \sqrt{R_{s,max} R_{s,min}} \tag{5}$$

Then, if the maximal output voltage range obtained is greater than that necessary to achieve the desired DR, we can reduce that voltage range by increasing R_1 or by reducing V_{ref}; both actions will reduce the power dissipated. However, to obtain a digital output independent from the particular value of V_{ref}, the ADC should use the same voltage reference, and therefore this should be selected close to the power supply voltage. The value of R_1, selected according to (5), will be high for resistive sensors that have high resistance values. Therefore, this design approach will yield a low power consumption for this kind of sensors.

For low-resistance sensors, such as RTDs, selecting R_1 according to (5) yields a large $P_s + P_i$. Therefore, to reduce power consumption it may be better to select a large R_1 and compensate for the reduced output voltage range by adding gain and improve DR by reducing noise (by adding filtering stages, for example). This approach should be also followed if the maximal range achievable with the interface circuit was smaller than that needed to meet specifications. Next the effect of gain and filtering stages in the total power consumption of the system is analysed.

2.2. Gain stage and filtering

Low-power amplifier ICs (op amps and instrumentation amplifiers) have been available for years [10]. Recent models have quiescent currents below 1 μA for op amps and 40-60 μA for instrumentation amplifiers yet have adequate dc voltage gains. For op amps, using high-value resistors in the feedback network keeps the overall power consumption small. Therefore, any reduction of the output voltage range in the sensor interface circuit to reduce power consumption in it can be compensated for by a gain stage which adds little power dissipation. The ultimate limits of this approach are the gain-bandwidth trade-off of the amplifier, which limits the maximal voltage gain, and the input voltage range allowed for the op amp, whose closeness to the power supply rails depends on technology. If the voltage coming from the interface circuit is too close to the lower supply voltage, the amplifier will not work. Low-power amplifiers and high-value resistors certainly increase system noise; resistors contribute white noise and op amps add white and $1/f$ noise. A filtering stage can reduce noise to an acceptable level, but filters will also dissipate power.

The steady-state power consumption P_f of a first-order low-pass *RC* filter is due to that of its resistor:

$$P_f = \frac{|V_R|^2}{R} \tag{6}$$

being V_R the voltage across it:

$$V_R = V_{in} \frac{jf}{jf + f_c} \quad (7)$$

V_{in} is the input signal, f is the frequency and f_c is the corner frequency of the filter. Substituting (7) into (6) yields:

$$P_f = \frac{V_{in}^2}{R} \frac{f^2}{f^2 + f_c^2} \quad (8)$$

From (8) we note that P_f tends to zero for signals in the filter pass band whose frequencies are well below the corner frequency f_c. Only signals, plus noise and interference, close to f_c and noise and interference in the stop band will dissipate some power. But for passive filters, power dissipated by noise and interference will be supplied by their sources, not by the power supply of the measurement system. In systems that include an active gain element (such as an amplifier) prior to a passive filter, noise and interference at the amplifier input will be amplified and their power, supplied by the system, will be dissipated in the filter. This is also the case for active filters, which are an alternative to merge the gain and filtering stages. In any case, the power of noise and interference is usually much smaller than that of the signal, so that it will not significantly contribute to the total power consumption. Furthermore, noise and interference can always be reduced by adding extra passive filter stages prior to the active gain stages. Therefore, gain and filtering stages are highly valuable low-power design blocks that can match voltage ranges while maintaining the desired dynamic range and without contributing too much to the overall power budget in (2).

2.3. A/D conversion and overall design guidelines

The dynamic range at the input of the ADC of a sensor-based measurement system that includes an interface circuit and a stage with gain G is:

$$DR = \frac{GV_{i_{FS}}}{\Delta V_a} \quad (9)$$

The resolution in voltage ΔV_a at the input of the ADC is determined by either that of the ADC (quantization interval or noise) or by the noise of the stages preceding the ADC. This noise can be reduced by additional filtering or by using low-noise amplifiers, but these have large quiescent currents (large P_a).

In summary, the desired DR in the signal chain can be obtained by designing an interface circuit with the maximal output voltage range (maximal sensitivity for the voltage divider) and a low-gain amplifier, or no amplifier at all, or by designing an interface circuit with a smaller output voltage range (smaller sensitivity) followed by an amplifier with a large-enough gain to compensate for the loss in sensitivity in the voltage divider. The optimal power design will be that that minimises P_T in (2) while ensuring that voltage ranges and levels are compatible.

3. MATERIALS AND METHODS

To study the usefulness of the proposed design guidelines for a specific resistive sensor, we compared power consumption for two signal conditioning approaches for a Pt1000 temperature sensor. The first approach was the classical approach of reducing power by minimising the number of parts. It consisted of a voltage divider with R_1 selected according to (5) to achieve the maximal sensitivity for the voltage divider, hence the largest output voltage range (Fig. 3). We selected the standard value R_1 = 1 kΩ as an approximation to the optimal value calculated from (5).

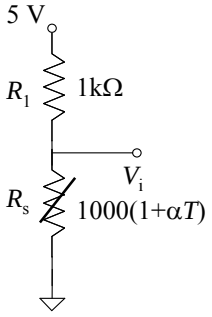

Fig. 3. Minimal interface circuit for a Pt1000 sensor.

For the second approach (Fig. 4), we sought to reduce the overall power consumption in the signal conditioning stages in (2). For this, we increased R_1 to 100 kΩ to reduce power consumption in the voltage divider, and added a voltage amplifier built from a low-power op amp (MAX4474, I_{supply} = 750 nA). We selected G = 50 to compensate for the reduced output range of the voltage divider and obtain a voltage output similar to that of the circuit in Fig. 3. We also added a first-order low-pass filter ($f_c \approx$ 1 Hz) to reduce the noise introduced by the additional components. We used a single supply voltage (5 V) in both circuits.

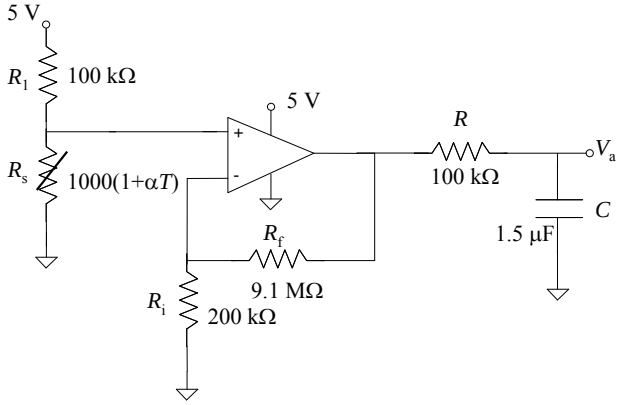

Fig. 4. Low-power signal conditioner for a Pt1000 sensor.

To assess the performance of the two circuits, we measured their output voltage and total current consumption using a 5½ digit digital multimeter (HP 3478A, 5 Hz bandwidth) at 20 ºC and 30 ºC set with a dry-well calibrator (Hart Scientific 9102S, ±0.25 ºC accuracy). For the output voltage measurements we averaged 50 readings. We

calculated the standard deviation to estimate the output noise. Noise bandwidth was determined by the digital multimeter in the first circuit and by the low-pass filter (1 Hz) in the second circuit.

In order to test the limits of the approach in Fig. 4, we performed a second experiment consisting in further increasing R_1 to 1 MΩ and to 10 MΩ. We increased the amplifier gain accordingly to obtain an output voltage similar to that in the previous experiment, by reducing R_i in Fig. 4 to 20 kΩ and 2 kΩ respectively.

4. EXPERIMENTAL RESULTS AND DISCUSSION

Total current consumption was I_{cc} = 2.4 mA for the simple voltage divider (Fig. 3) and I_{cc} = 54 μA for the circuit designed according to the optimal power guidelines (Fig. 4), hence about 45 times less. The amplifier and filter consumed only 10 % of the current in the second circuit, hence corroborating their low power consumption.

Table 1. Average of 50 readings and standard deviation for the output voltages of circuits in Fig. 3 (V_i) and Fig. 4 (V_a).

	T = 20 ºC	T = 30 ºC
V_i/V	2.56867	2.61709
σ_i/V	0.00036	0.00035
V_a/V	2.83427	2.92687
σ_a/V	0.00025	0.00027

Table 1 shows the averaged output values and standard deviations for the two circuits. The output sensitivity for the voltage divider in Fig. 3 was about 5 mV/°C whereas that for the circuit with reduced power dissipation (Fig. 4) was about 9 mV/ºC (including the amplifier gain, G = 46.5). Both circuits have similar standard deviations for the output voltage, which, using a coverage factor of 2, imply approximate temperature resolutions of 0.14ºC and 0.06ºC respectively, both better than the accuracy limit of the temperature calibrator used and close to the accuracy limit for platinum RTDs. The slightly smaller standard deviation for the second circuit can be explained from its smaller noise bandwidth. In addition to its lower power consumption, the second circuit, with a higher R_1, is more linear [7] and, as the current that flows through the RTD is much lower, has a reduced self-heating of the sensor.

These results corroborate that reducing the number of parts does not necessarily reduces power consumption in the system. Therefore, considering power reduction in the measurement chain as a whole rather than in individual components can improve power performance. As for the cost, the added components are inexpensive and their upfront cost must be compared with the benefit of an extended life for batteries, or power bills for systems that run continuously. For systems whose power supply is turned on only when measuring, the energy spent in charging the circuit capacitances should be considered.

Table 2. Average of 50 readings and standard deviation for the output voltages of circuit in Fig. 4 with R_1 = 1 MΩ.

	T = 20 ºC	T = 30 ºC
V_a/V	2.30638	2.40954
σ_a/V	0.00142	0.00159

Table 2 shows the effect of further increasing R_1 to reach the minimal power consumption achievable with the design approach in Fig. 4. Using R_1 = 1 MΩ reduces the total current consumption to 6.6 μA at the cost of amplifying the noise in the circuit (due to the resistors and the op amp) by a higher gain (G = 456), hence worsening temperature resolution to 0.15 ºC. We also observed a reduced output voltage with respect to that when R_1 = 100 kΩ. This reduction can be attributed to the op amp input offset voltage (about -0.5 mV), which added perceptibly to the reduced output of the voltage divider (which was about 5 mV for the R_1 selected). As R_1 was further increased to 10 MΩ, the output of the voltage divider became too close to the lower supply voltage of the amplifier to yield a significant output in the circuit. This limitation could be overcome by using an amplifier with rail-to-rail input. Nevertheless, for such high values of R_1, the power consumption due to the voltage divider would become comparable to that of the amplifier. Therefore, a much less significant power reduction would be achieved in exchange for the increased noise due to the higher gain.

The fact that when selecting $R_1 >> R_s$ the output of the voltage divider is very close to 0 V, is another advantage of the proposed approach. When designing voltage dividers for maximal sensitivity, their output voltage is centred around $V_{ref}/2$. This offset can be cancelled out by high-pass filtering but for very low-frequency measurements this becomes impractical. The common solution is to design a Wheatstone bridge by using another voltage divider whose output remains constant, and measure the difference between the two voltage dividers. But this additional voltage divider doubles the power consumption of the interface. Hence, for low-power design, Wheatstone bridges should be used only when the sensor includes two or more resistive sensors. If the two sensors are in different branches, for example to measure a difference, the constant-value resistors in the two other arms can be selected to have a low-power dissipation, and the loss in sensitivity can be compensated by additional gain in the ensuing amplifier.

The high-resolution digital multimeter used to measure the output voltage in Figs. 3 and 4 overcame the need of the ADC in Fig. 1 and provided a fast method to assess the power reduction obtained with the proposed design method. But it must be pointed out that the resolution needed for the ADC will depend on the previous signal conditioning and attempts to reduce power consumption by using a minimal signal conditioner (no amplifier) can backfire because, for a given sampling speed, power consumption increases with resolution. Therefore, if an amplifier will be used anyway, it is better to design the largest gain allowed by its gain-bandwidth product, and reduce the sensitivity of the voltage divider.

5. CONCLUSIONS

We have analysed the power consumption of the functional blocks of a sensor-based measurement system to determine the optimal power design for a given dynamic range of the measurand. The analysis shows that minimising the total power consumption in the measurement chain can lead to design solutions that do not imply a minimal number of components in the system.

For high-resistance sensors, a simple voltage divider can be the best option provided that its output voltage range suits the input voltage range of the ADC and this one has a large-enough resolution.

For low-resistance sensors, the best option is to reduce power consumption as much as possible in the interface circuit (voltage divider), and use a low-power gain stage to compensate for the lower sensitivity of the voltage divider. To reduce the higher noise due to low-power op amps and higher resistor values in their feedback loop, a filtering stage can be used without significantly increasing the total power consumption of the system This approach is limited by the gain-bandwidth trade-off in common voltage amplifiers, which is especially restrictive for low-power op amps, and by the input voltage range of the op amp used, as the voltage divider voltage can become too close to the lower supply voltage, preventing the amplifier from working properly if it does not have a rail-to-rail input capability.

We have experimentally verified the design approach for low-resistance sensors for a Pt1000 sensor. Current consumption reduces from 2.4 mA in the voltage divider designed for maximal sensitivity to 6.6 μA when increasing the value of the other resistor in the voltage divider and adding a low-power gain stage and a passive low-pass filter to compensate for the sensitivity loss in the voltage divider. The resolution is similar in both circuits, although it becomes worse in the low-power circuit as we increase the amplifier gain. Therefore, there is a trade-off between power consumption and measurement resolution in the design approach proposed. The low power circuit is more linear and has a reduced self heating as compared with the voltage divider designed for maximal sensitivity.

This approach can also be applied to the design of Wheatstone bridges with two sensors in different branches. Wheatstone bridges with a single sensor consume more power than a voltage divider designed according to the proposed method and offer no major advantage.

Future work will include using additional sensors, such as high-resistance NTC thermistors, and half- and full-bridge sensors (piezoresistive and magnetoresistive) and the instrumentation amplifiers associated to them, as well as a complete analysis of the measurement chain when additional functions such as voltage level shifting is considered for an ADC that has the minimal resolution needed for the application in hand.

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