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REMOTE LABORATORY FOR FPGA BASED RECONFIGURABLE SYSTEMS TESTING

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Abstract – The paper presents a remote laboratory system that allows performing experiments controlled across the Internet via web interface as well as locally in the classroom. The system has been developed for courses of advanced digital design and signal processing using complex Field Programmable Gate Array (FPGA) platforms. It allows students full access to laboratory equipments, advanced software licenses, and FPGA platforms remotely using any common web browser and standard remote desktop interface. The system consists of Altera development FPGA kits and suitable instrumentations (Logic Analyser, Digital Oscilloscope, and Vector Signal Generator) or low cost alternative (DAQ board as a Virtual Logic Analyser, Oscilloscope and Vector Signal Generator). Both solutions use PC running an interactive LabVIEW based software including a Graphical User Interface (GUI).

Keywords: remote laboratory, FPGA hardware experiments, LabVIEW

1. INTRODUCTION

Training in advanced courses of Programmable Logic Devices (PLDs) requires access to expensive hardware equipments. The high cost of these instruments along with time consuming development process in individual students' projects required within the educational process creates a significant bottleneck. The restricted university budget does not allow building of a several such development and test stands, and time schedule and university security conditions restrict the time when the stand can be accessible for students locally in a laboratory.

A solution of this problem could be to build a remote laboratory. A virtual laboratory is generally based on sets of software models that represent objects or systems in a given abstraction level but its disadvantage is in accuracy of the behaviour model representing a real system and the speed of detailed simulation for complex systems. Unlike virtual laboratories, remote laboratories are based on real hardware [1], [2], [3], [4]. Such laboratories are very convenient and effective for hardware design laboratory courses and advanced hardware projects solved by students. Hardware experimental environment is usually treated as an exclusive resource for single user usage. However, the actual test run time is rather short and most of the time is wasted leaving these costly resources idle. The combined use of FPGA/PC connected test hardware and PC controlling measurement equipments such as Logic Analyzer (LA), Digital Storage Oscilloscope (DSO) and Vector Signal Generator (VSG) can represent an environment for remotely controlled hardware experiments.

The less costly second variant of the solution with the virtual instrument is nearly the same; the difference consists in replacement of standalone instruments performed by LA, DSO, and VSG by a DAQ. The LabVIEW drivers will be adapted to this solution. The price for this solution is a reduced possibility to measure transient effects on the programmed FPGA circuits. However, for introductory courses this solution is fully sufficient but the closeness to the simulation is its drawback.. The design of the fully equipped laboratory will be aimed first of all to advanced students, thesis works, and research. In the next paragraphs this fully equipped working environment as the most advanced solution will be described in further.

An example of such a remote laboratory system used in practice is Nokia Remote Device Access (RDA) [4]. It is a service that allows developers to test their mobile applications and services remotely on various Nokia devices based on Symbian OS. The main features of the service are remote controlling of a device, installing and running applications, transferring files, and analyzing log files in real-time. RDA is an Internet-based solution.

The aim of this paper is to describe hardware (HW) and software (SW) tools necessary for building of a remote web-based laboratory targeted at advanced FPGA development and testing for educational and research purposes at the Department of Electronics and Multimedia Communications, Technical University of Kosice.

2. DESIGN OF REMOTE LABORATORY SYSTEM ARCHITECTURE

The main idea behind the project is to provide an access to the really expensive HW and high performance licensed EDA tools, and to enable using these costly resources remotely via Web access and remote desktop interfaces. Basic structure of the laboratory which consists of stand

alone instruments controlled remotely (first variant) is shown in Fig. 1.

The core of the system consists of:

- Web and Measurement Servers with LabVIEW based control software,
- a set of Altera FPGA Development Kit boards,
- Agilent 16822A Logic Analyzer - 68 Ch 4 GHz Timing 500 MHz State Logic Analysis, with 48 Channel Pattern Generator,
- Tektronix TDS2004 4-channel Digital Storage Oscilloscope ,
- Anritsu MG3700A Vector Signal Generator ,
- EDA tools Application Server DELL 690 workstation, 4-core Xeon CPU, 8 GB memory.

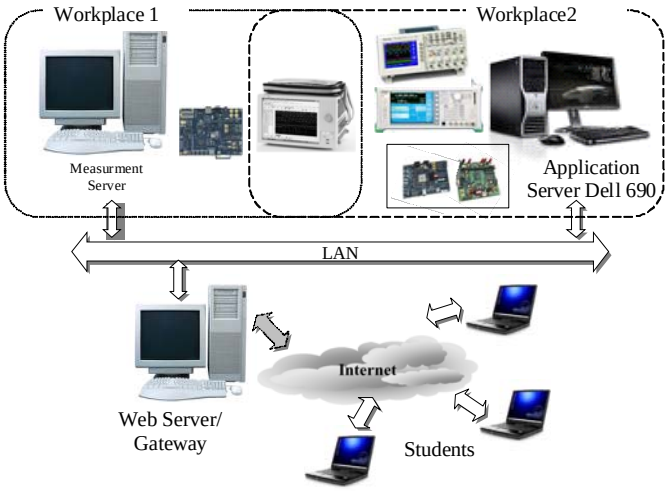

Fig. 1. Architecture of the proposed remote laboratory.

The measurement instrumentations (LA and VSG) are linked to the Measurement Server via LAN (Ethernet) that creates the local communication backbone. The DSO vendor has implemented into DSO only USB, that is why the communication with DSO has to use this interface. From the measurement point of view the main bottleneck of the Ethernet and USB is the precise group triggering and synchronization in the measurement system in comparison with optional GPIB (IEEE-488) but no extreme triggering requirements are expected in the suggested system. Moreover, the local LAN is not overloaded by general communication what decreases possibility of any delays in control command delivery.

The instruments serve for two independent measurement stands:

- Digital electronics test stand that enables performing tests on FPGA equipped with LA with build-in pattern generator.
- Mixed analogue and digital electronics test stand that enables performing tests on digital signal processing (DSP) and video kits equipped with VSG and DSO.

2.1. Software for control of test stand instrumentation

The software has to fulfill the following requirements:

- To control the instrumentations according to the requirements of a user.
- To acquire measured data from LA and DSO, to process and prepare it for delivery to the end user in a convenient format, e.g. graph, listing, data file, etc.
- To accept, process, and upload user data to the pattern and arbitrary generators.
- To run, trigger, and synchronize the performance of the current measurement task.

LabVIEW by National Instruments [17] has been chosen as the software development platform for these software applications. The main reasons leading to this decision were:

- Simple graphical programming environment that enables rapid and effective development of an application for measurement and signal processing. It is easy to learn and is supposed to be a standard in the measurement system programming. This fact opens a way how to attract and involve also skilled students into the development of some remote laboratory components, e.g. within their theses, etc.
- Simply applicable instrument drivers offered by the instrument vendor and National Instruments that significantly simplify the programming.
- Integrated functions for Internet data transfer using various data transfer protocols and built in Web Server.
- Rich libraries for data processing and analysis.

The software consists of two sets of independent applications for FPGA and DSP based kits, respectively. These applications have to enable the students to have a complex and comprehensive view of performed measurement task and a possibility to set up the conditions of measurement simply, e.g. parameters of stimulus signal, etc. The required simplicity is the reason why the control of instrumentation was partially restricted to the functions that are really needed for the given tasks. Moreover, to allow remote controlling of the instrumentations across the Internet, specialized software tools implemented on the Measurement Server had to be developed.

The instruments drivers developed by vendors unfortunately use different methods of data/command transfer among the Measurement Server and the instrument itself. The LA by Agilent requires communication based on COM automation objects, methods, and properties programming, while DSO by Tektronix and VSG by Anritsu use common VISA-based access. To simplify the complex programming even using the instrument drivers we decided to use only a restricted variety of COM automation components to transfer the configuration XML-based file that is edited on the Measurement Server according to user measurement requests and measurement data files.

The proposed HW infrastructure provides an access to expensive HW in time multiplex (job scheduler) [2], [3]. It should enable to a remote user to load his/her FPGA project via web interface into a buffer where it would wait in a time front when the HW resources will be freed. As soon as the HW is available, the job is processed and the results of HW responses are sent back to the user for off-line analysis of the testing results.

Basic features expected of the job scheduler are:

- Automatic submission of executions.
- Interfaces to monitor the executions.
- Priorities and/or queues to control the execution order of unrelated jobs.

Job scheduling enables seamless access to the HW and SW resources to several concurrent users. It enables more effective use of the HW equipments.

3. REMOTE LABORATORY WORKPLACES

The remote laboratory consists of the two workplaces:

1. Workplace for basic FPGA designs
2. Workplace for DSP IP Blocks Based Design Testing

3.1. Workplace for basic FPGA designs and soft processor testing

Workplace 1 provides access to the NIOS II Development Kit, Cyclone II Edition (ALT1) and LA with pattern generator functionality (Fig. 1). The ALT1 kit is based on the low-cost Altera Cyclone II EP2C35F672 FPGA device (Fig. 2) that is used in many typical cost sensitive applications. It is connected via Altera download cable - USB blaster [6] directly to the Measurement Server.

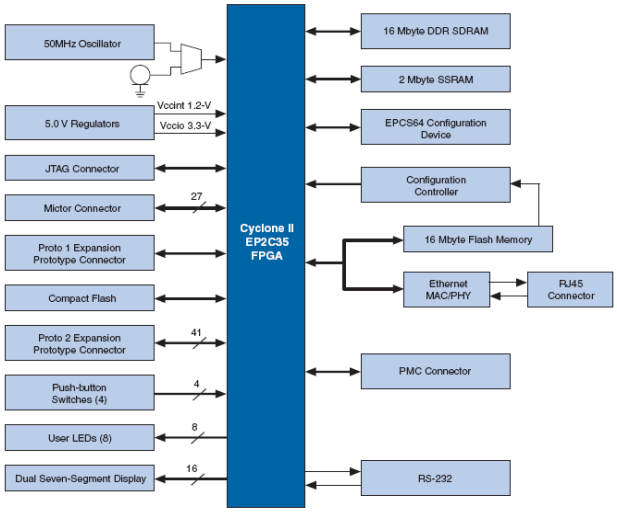

Fig. 2. NIOS development board, Cyclone II edition block diagram.

The USB-Blaster download cable interfaces a USB port on the Measurement Server to the Altera FPGA mounted on a printed circuit board. The cable sends configuration data from the remote user to a standard 10 pin JTAG header connected to the Cyclone FPGA. LA is connected to the selected measurement points of the Cyclone FPGA device and NIOS II board buses. LA is used mainly for capture of FPGA responses during testing phase. Pattern generator of LA can be optionally used for generation of user definable digital stimulus sequences. It can be even controlled remotely through remote programming interface (RPI) by issuing ASCII commands to the TCP socket.

The Workspace 1 supports standard iterative FPGA design and testing flow and provides HW platform for the following types of experiments:

- Development and testing of general digital logic designs. All EP2C35 Cyclone FPGA device resources (logic elements, embedded memories, PLLs, etc.) are available to the remote user. Such designs can vary from very simple up to complex standalone designs.
- Development and testing of designs based on the predefined standard soft 32-bit RISC NIOS II processor [7] designs. All NIOS II board resources (FLASH, SDRAM, UART, Compact FLASH, …) are available to the remote user. Quite complex hardware and software designs can be tested (e.g. embedded uClinux based applications) with relatively small user design effort. They can clearly demonstrate advantage of FPGA usage and Intelectual Property (IP) blocks based design approach in modern embedded applications.
- Development and testing of NIOS II based designs extended with custom peripherals [13] embedded into EP2C35 Cyclone FPGA device. Such designs represent the most complex designs based on hardware/software co-design.

3.2. Workplace for DSP IP Blocks Based Design Testing

Workplace 2 (Fig. 1) enables access to the DSP Development Kit, Stratix Edition [8] and Video Development Kit, Cyclone II Edition [9]. These kits provide target FPGA platforms for testing DSP functionality of modern FPGA devices. Both Altera FPGA devices (Stratix II EP2S60F1020C4 (Fig. 3) and Cyclone II EP2C70F672C6) contain embedded multipliers that are crucial for embedded DSP.

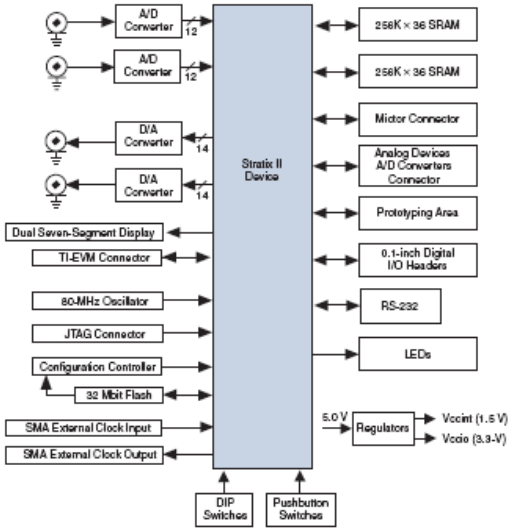

Fig. 3. Stratix II EP2S60 development board block diagram.

The kits offer the following analog interfaces:

- Two 12-bit (14-bit), 125-million samples per second (MSPS) analog-to-digital (A/D) converters.
- Two 14-bit, 165-MSPS digital-to-analog (D/A) converters.
- VGA digital-to-analog converter (DAC).

These interfaces together with the high performance FPGA resources allow testing of quite complex DSP algorithms embedded into FPGA devices. DSP designs based on available Altera IP blocks are the typical designs tested on Workplace 2. Design flow of the characteristic IP

based designs are supported by the licensed Altera Quartus II [10] EDA tool, selected IP Megafunctions supported by Altera DSP Builder [11], and Matlab running on the Application Server. Access to these resources is performed by standard remote desktop access with dynamic access control implemented on the Web Server.

Powerful VSG can be used for generation of complex synthesized analogue waveforms used in common testing DSP applications. Waveform generation can be based on predefined waveforms stored on the VSG hard disk or user defined by using Matlab tools. The 4-channel DSO can capture analogue waveforms generated by testing DSP applications. Both of the measurement equipments can be controlled by the Measurement Server and the captured data can be sent to the remote user for further off-line analysis.

The Workspace 2 supports advanced DSP IP block FPGA design and testing flow shown and provides HW platform for the following types of experiments:

- Development and testing of Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters embedded into target FPGA devices.
- Testing of real time processing of selected digital modulation (AM, FM, OFDM, etc.) A set of predefined experiments will be used as a standard HW testing approach.
- Basic processing and generation of video signals. A set of predefined experiments will be used as a standard HW testing approach.
- Development and testing of custom DSP applications. Due to the complexity of such designs, it is expected that these will be performed within Master and, in particular, PhD theses

These experiments allow filling the gap among specialized theoretical subjects given at the Department of Electronics and Multimedia Communications, TU Kosice, and functionality of current modern FPGA devices. IP based development of DSP applications enables to build up quite powerful applications with reasonable development effort. It can also increase motivation of students to follow this rapidly evolving branch of the study more deeply.

4. SOFTWARE TOOLS AVAILABLE TO REMOTE USERS

Standard FPGA designs can be done off-line by free Altera EDA Quartus II tool [10]. This tool is available free off charge and a remote user can download and license this software for local usage. Designs for the both of Cyclone boards can be done with this software.

The powerful DELL Application Server with remote desktop access was added in order to support also more advanced designs with licensed software tools available at the Department of Electronics and Multimedia Communications:

- Fully licensed Altera Quartus II EDA tool provides a possibility to use also Altera Stratix FPGA based designs.
- A set of licensed Altera IP blocks can be used for building advanced DSP based applications.
- Nios II C-to-Hardware Acceleration Compiler [12] can be used for automatic C to hardware transformation.
- Matlab simulation environment can be used e.g. for definition of custom waveforms or other advanced DSP experiments.
- Matlab Signal processing toolbox can be used for simulation of advanced DSP applications.
- Filter Design Toolbox can be used for design of FIR and IIR filter parameters.
- EDA Simulator Link™ MQ for Mentor Graphics Modelsim [14] can be used for high-level connection of Matlab with Modelsim simulation environment.
- High performance Modelsim simulator [14].

These tools are currently fully licensed for educational and research purposes at the department and access to them will be controlled by access policy implemented on the Web Server/Gateway. These tools represent current state of the art for design and testing of modern embedded FPGA based designs with Altera FPGA devices. Remotely accessible Application Server enables to use this advanced technology within standard educational and research activities.

5. CONCLUSIONS AND FUTURE WORK

The paper presents some aspects of the remote FPGA laboratory for development and testing of complex reconfigurable systems which is being built up at the Department of Electronics and Multimedia Communications at the Technical University of Kosice. The laboratory is still in the process of development. Basic functionality of the Workspace 2 was already successfully tested during development of video signal processing based on IP functions [15]. This HW oriented diploma work used the main components of the proposed remote laboratory for

a) Debugging of HW based design of the custom video input/output extension board shown in Fig.2.
b) Remote access of data from LA connected to selected points of the developed board and Santa Cruz connector (Fig. 4).
c) Remote access to the licensed Altera IP functions and Quartus EDA tool by using the powerfull DELL application server.

Fig. 4. Custom extension video I/O board with SANTA CRUZ connector developed in [15] attached to the standard Altera video development kit.

This pilot diploma thesis fully confirmed advantages of availability to share remotely advanced HW and SW tools for real development works.

Currently, all equipments and evaluation boards are already fully functional and basic connectivity of the equipment is under testing. Although complete functionality of this remote laboratory is still not attained in the full scale, integration works are going to continue in the next months mostly as a part of specialized diploma works and PhD theses. Simultaneously also typical FPGA based experiments are prepared for demonstration of advantages of the modern FPGA devices for up to date embedded and DSP applications.

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