A SIMPLE FAULT DIAGNOSIS METHOD FOR ANALOG PARTS OF ELECTRONIC EMBEDDED SYSTEMS

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Abstract - A new simple method of single soft fault detection and localization of analog parts in embedded electronic systems controlled by microcontrollers is presented. In the pre-testing stage of the method a fault dictionary is created based on the map of localization curves. In the measurement stage the time response to a stimulating square impulse of the analog part is applied to the input of the analog comparator, and measurements of duration times of subsequent impulses of output signals of the analog comparator are realized by the internal timer of the microcontroller. In the last stage, fault detection and localization are performed by the microcontroller. The main advantage and novelty of the method is the fact that the BIST consists only of one analog comparator and two timers of the microcontroller already mounted in the system. Hence, this approach simplifies the structure and design of BISTs, which allows to decrease test costs.

Keywords: fault diagnosis, self-testing, BIST

1. INTRODUCTION

Nowadays, electronic devices usually in the form of electronic embedded systems, that is the systems with "embedded intelligence", are applied in almost all spheres of human life. E.g. in: medicine, motorization, multimedia, aviation, telecommunication, etc. It is important that these systems should work faultlessly. Thus, according to present tendencies these systems should self-test all their important functions.

Self-testing procedures of these systems regard to functional testing of the whole system [1], the software testing [2,3] and testing of particular blocks of the system [4]. One of these blocks, often applied in the embedded systems, is an analog part which is used mostly to adjust input analog signals usually coming from sensors and passed on to analog-to-digital conversion blocks.

Self-testing of analog parts should base on fault diagnosis methods of analog circuits with limited computational possibility of the embedded system. Hence, simulation-before-test methods are often used. Additionally, measurements of proprieties of the analog part can be realized only by blocks called Built-In Self-Testers (BISTs) additionally implemented in the system. In many cases the analog parts are used as amplifiers and aliasing filters for ADCs. For them generally three types of BISTs are used:

- Consisting of ΣΔ modulators, low-pass analog filters, ADCs, DACs and digital blocks [5,6].
- Using the oscillation-test methodology [7,8]. In this case the analog circuit is transformed into an oscillator by adding a feedback path and modifying the circuit either adding or removing some passive components. Additionally a digital circuit, which measures deviations of the frequency of oscillation of the tested circuit, should be built into the BIST.
- Built according to the test strategy based on power spectral analysis [9], where the tested circuit is stimulated by a noise generator, its response is sampled by an ADC and the estimation of the power spectrum density based on the fast Fourier transform is realized by a DSP microprocessor.

The BISTs mentioned above characterize hardware excess and great requirements relating to computing power. That causes increased production costs of the systems. Hence, the author proposed new solutions of BISTs in which the BISTs are created from already existing resources of embedded electronic systems, especially internal peripherals of control units (microcontrollers, DSPs). Additionally, these control units realize self-testing procedures of the analog part. In these solutions the analog part is stimulated by a sinus wave [10], a square wave [11] or a square impulse [12] generated by e.g. a microcontroller and the circuit response is sampled by the internal ADC of the microcontroller [11,12] or it is converted to digital signals (with duration times measured by the internal timer of the microcontroller) by a set of analog comparators with different threshold voltages [13]. Such approaches allow to minimize the test cost and guarantee a high quality of products.

However, in the paper a new simple method of single soft fault diagnosis for analog circuits is proposed. It allows to considerably simplify the construction of BISTs proposed in [13] and it is more suitable for diagnosis of third-, fourth- or higherorder analog filters. Also, a new methodology of creation of the fault dictionary data used by the fault detection procedure and a new measurement procedure are presented.

2. DESCRIPTION OF THE METHOD

The description of an implementation of the fault diagnosis method will be illustrated on the example of the embedded system controlled by the ATmega16 microcontroller (Fig. 1). The Timer 2 of the microcontroller is responsible for generating the square stimulating impulse,

the single analog comparator converts the response of the analog circuit into a set of consecutive one-by-one square impulses whose duration times are measured by the Timer 1.



Fig. 1. Example of the electronic embedded system in self-testing configuration of the analog part.

Hence, the microcontroller controls its timers, that is the reconfigurable BIST, according to the measurement procedure included in its program memory, and it also runs fault detection and localization procedures. Thus, as it is shown in Fig. 1, the BIST consists of only internal timers of the microcontroller and only one analog comparator with one setting value of the threshold voltage in opposition to the method proposed in [13], where we used K analog comparators and each of them had different values of the threshold voltage.

As an example of the analog part, the Tow-Thomas filter was chosen (Fig. 2).



Fig. 2. Tested analog circuit – low-pass Tow-Tomas filter, where $R1 = R2 = R3 = R4 = R5 = R6 = 10 \text{ k}\Omega$, C1 = 33 nF, C2 = 6.8 nF.

2.1. Idea of the method

If we stimulate the analog part (Fig. 2) by a single square impulse (with a duration time $T = 568 \,\mu$ s), we receive an analog response which passes several times the zero voltage level, as shown in Fig. 3.

When we let these responses through the analog comparator with threshold voltage $v_{threshold}$ ($v_{threshold}$ is set to 50 mV) as shown in Fig. 1, we obtain a set of digital impulses with different duration times τ_k , k = 1, ..., K, where K is the number of successive impulses taken into consideration (Fig. 3). These times represent moments at which the analog response for the given value of particular elements is above the threshold voltage. They are different for respective elements, thus these times we can subordinate to the particular elements, that is we can use them for fault localization.



Fig. 3. Time responses of the analog circuit (Fig. 2) for the 0.5 nominal value of the respective element (remaining elements have nominal values), and digital signals at the output V_{comp} of the analog comparator.

Fig. 4 shows sets of time responses to the square impulse of the analog circuit from Fig. 2 for changes of values of all elements from 0.1 to 10 of their nominal values.



Fig. 4. Sets of time responses of the Tow-Tomas filter (Fig. 2) for changes of values of all elements from 0.1 to 10 of their nominal values.

It is seen that the responses of the circuit for the assumed range of change of elements for different elements do not fall on each other. Therefore it is possible to discern and to assign these responses to given elements or given ambiguous groups and also to their given values.

Let us assume that the analog circuit consists of *I* passive elements and τ_k^{il} is the duration time of the *k*-th impulse (where k = 1, ..., K, and we assumed K = 3) of the output signal V_{comp} of the analog comparator for the *i*-th element, i = 1, ..., I, and l = 1, ..., L, where *L* is the assumed number of discrete values of the *i*-th element within a range from $0.1p_{i nom}$ to $10p_{i nom}$ ($p_{i nom}$ – the nominal value of the *i*-th element).

Fig. 5 presents converted sets of timings shown in Fig. 4 by the analog comparator. It is seen from Fig. 5 that for each *i*-th element the output signals from the analog comparator

are different. They have different duration times τ_k^{il} according to the *l*-th value of the *i*-th element and the number *k* of the next impulse. So we can assign these duration times $\{\tau_k^{il}\}_{k=1,...,K, i = 1,...,l}$ of output impulses to the given element and also its particular values.



Fig. 5. Sets of digital signals at the output V_{comp} of the analog comparator for changes of values of particular elements from 0.1 to 10 of their nominal values.

Therefore, we can create a measurement space where the first coordinate will be represented by the duration time τ_1 of the first pulse, the second coordinate by the duration time τ_2 of the second pulse, etc. Thus, for K = 3 we obtain the $\tau_1 - \tau_2 - \tau_3$ measurement space.

Hence, we can treat the sets $\{\tau_k^{il}\}_{k=1,...,K, i=1,...,L, l=1,...,L}$ as the sets of coordinates $\{(\tau_1^{il}, \tau_2^{il}, \tau_3^{il})\}_{i=1,...,L, l=1,...,L}$ of p_{il} points. Thus, we can place these points into the measurement space (see Fig. 6). In this case, they compose *I* localization curves, where each *i*-th curve is represented by the set of $\{p_{il}\}_{l=1,...,L}$ points. That is, in this way we transform the sets of duration times shown in Fig. 5 into a family of localization curves placed in the measurement space (Fig. 6). Thus, we can say that each curve describes the behaviour of the circuit following a deviation of value of the particular element.

As described in [11,13] and in this case we can illustrate the fault localization in a graphical way. Thus, the fault localization consists in putting the measurement results of duration times treated as the measurement point p_{meas} with coordinates (τ_1^{meas} , τ_2^{meas} , τ_3^{meas}) into the measurement space $\tau_1 - \tau_2 - \tau_3$ (Fig. 6). Appurtenance of the p_{meas} to the adequate curve locates the faulty element.



Fig. 6. Map of localization curves for the tested circuit (Fig. 2) in the 3-dimensional measurement space.

Hence, this map of localization curves is a graphical representation of the fault dictionary of the circuit.

The argument presented above can be expressed by the following transformation:

$$T_i(p_i) = \sum_{k=1}^{K} \tau_k^i(p_i) \mathbf{i}_k \tag{1}$$

where: \mathbf{i}_k - is a coordinate vector along the *k*-axis, k=1, ..., K, $\tau_k^i(p_i)$ – the value τ_k^i of the duration time of the *k*-th impulse of the output signal of the analog comparator for the p_i value of the *i*-th element.

2.2. Improvement of the localization resolution

The localization resolution depends on the shape of the curves and their mutual locations. If the curves are more separated and they have greater similar length, the localization resolution grows. Thus, it is important to determine the parameters which improve this resolution. For this method we can manipulate only two parameters: the duration time of the stimulating square impulse T (the amplitude is set a priori to V_{cc}) and the threshold voltage $v_{threshold}$ of the analog comparator.

The duration time T of the stimulation should be set to a value for which the responses of the analog circuit have the greatest possible dynamics, that is e.g. they pass many times through the threshold voltage level and the duration times of next impulses at the output of the analog comparator are possibly differing.

Thus, we propose to assign the duration time of the stimulating square impulse in two steps. In the first step this time is set to a half of the value $T_c = 1/f_c$, where f_c is the cutoff frequency of the analog part (Fig. 2). Hence, we operate in the bend of the frequency characteristic, that is in the place for which the circuit functions are the most sensitive to changes of element values. In the second step we fit the duration time T in a simulated way to obtain the greatest possible dynamics of changes of duration times τ_k^i . To analyze the influence of the threshold voltage $v_{threshold}$ on a distribution of localization curves, we introduced the coefficient κ^{i}_{k} equal to the difference between maximum and minimum values of the duration times τ^{il}_{k} of the *k*-th impulses of the responses the analog comparator analyzed for changes of *i*-th element values in the assumed range. It can be treated as the equivalent of high signal circuit sensitivity. It has the following form:

$$\kappa_k^i(v_{threshold}) = \max_{l=1,..,L} \left(\tau_k^{il}(v_{threshold}) \right) - \min_{l=1,..,L} \left(\tau_k^{il}(v_{threshold}) \right)$$
(2)

Basing on this coefficient we defined a coefficient κ^i describing the influence of the *i*-th element value changes on the dynamics of changes of all duration times:

$$\kappa^{i}(v_{threshold}) = \frac{1}{K} \sum_{k=1}^{K} \kappa^{i}_{k}(v_{threshold})$$
(4)

Hence, it specifies the influence of the *i*-th element on the circuit function, that is in our case what is the length of the *i*-th curve. Thus, it is required that this coefficient should be possibly the greatest.

By averaging these coefficients κ^i for all *I* elements we obtain the κ coefficient:

$$\kappa(v_{threshold}) = \frac{1}{I} \sum_{i=1}^{I} \kappa^{i}(v_{threshold})$$
(3)

Thus, it describes an averaging influence of all circuit elements on the circuit function. Hence, it describes the "quality" of the distribution of the localization curves. If κ is greater, then the mutual arrangement of the curves is better. Hence, also the localization resolution is better.



Fig. 7. Charts of κ coefficients for the tested circuit (Fig. 2) in function of the threshold voltage $v_{threshold}$ of the analog comparator.

Thus, we should chose the maximum value of the κ coefficient:

$$\kappa_{\max} = \max_{j=1,\dots,J} \kappa_k \left(v_{threshold}^j \right)$$
(5)

Basing on this value we determine the threshold voltage $v_{threshold}$: $\kappa_{max} \rightarrow v_{threshold_max}$.

Fig. 7 shows charts of these coefficients. It is seen that the maximum values of κ^i and κ are for the threshold voltage $v_{threshold}$ closing in to 0 V.

This analytical argument confirms the fact that the threshold voltage $v_{threshold}$ should be close to 0 V, because it allows to convert signals taking into account the whole range of their value changes above 0 V, and also small signals, what is important for fast- disappearing signals.

But the value of the threshold voltage $v_{threshold}$ should be above the level of noise and disturbances. Therefore it is one reason for which this value should be greater from 0 V.

3. THE FAULT DICTIONARY

The fault dictionary is created in a pre-testing stage. It consists of data used to fault detection and data used to fault localization.

The detection part data of the fault dictionary consists of coordinates of the nominal point p_{nom} with coordinates $(\tau_1^{nom}, \tau_2^{nom}, \tau_3^{nom})$ and the value τ_{ε} defining the radius of a sphere approximating the nominal area. The value τ_{ε} is determined according to the following algorithm:

• *M* points $\{p_m\}_{m=1,...,M}$ with coordinates $(\tau_1^m, \tau_2^m, \tau_3^m)$ representing the nominal area are generated using the Monte Carlo method (Fig. 8).



Fig. 8. The set of points representing the nominal area for the tested circuit (Fig. 2) in the 3-dimensional measurement space.

• Next *M* distances $\{d_m\}_{m=1,..,M}$ between these points and the nominal point p_{nom} are calculated:

$$d^{m} = \left\| \left\{ \left(\tau_{k}^{m} - \tau_{k}^{nom} \right) \right\}_{k=1,\dots,K} \right\|$$
(6)

where $\|\cdot\|$ is the norm defining distance between two points in the *K*-dimensional space. We assumed the taxi norm which bases on simple calculations, and thus it needs small computing power.

• From the set $\{d_m\}_{m=1,..,M}$ the maximum value of the distance d_N is determined, where we marked by N the assumed number of intervals of distances values (the number of bars) for the distance histogram (Fig. 9):

$$d_{N} = \max_{m=1,\dots,M} \left\{ d^{m} \right\} \tag{7}$$

• Basing on this value the values of ends d_n of all N intervals (bars) are calculated:

$$d_n = n \cdot \frac{d_N}{N} \tag{8}$$

• Next, we generate the histogram shown in Fig. 9. It presents distribution of quantity of distances regard to their values. Thus, each *n*-th bar presents M_n distances d^m (the number of elements of the set $\{d^m\}_{m=1,..,Mn}$) which are comprised in $d_{n-1} < d^m \le d_n$.



Fig. 9. Histogram for distances $\{d^m\}_{m=1,...,M}$ between points of the nominal area $\{p^m\}_{m=1,...,M}$ and the nominal point p^{nom} for the tested circuit (Fig. 2).

- Next, we assume the probability ε of belongings the p_m points to the nominal area (we assumed $\varepsilon = 99.73\%$).
- Basing on the ε coefficient we determine the value N_{ε} for which are simultaneously fulfilled the inequalities:

$$\sum_{n=1}^{N_{\varepsilon}-1} M_n < M \cdot \varepsilon \quad \text{and} \quad \sum_{n=1}^{N_{\varepsilon}} M_n \ge M \cdot \varepsilon$$
(9)

where $N_{\varepsilon} \leq N$ and $M = \sum_{n=1}^{N} M_n$.

The value N_ε points the d_{nε} value defining the radius of the approximation sphere of the nominal area for given ε. Finally we mark this value by τ_ε.

The data used by the fault localization procedure are generated basing on the map of localization curves (Fig. 6). To generate of descriptions of curves placed in the 3-D space taking into account element tolerances we can use the algorithm described in [13]. In this case the *i*-th curve is represented by:

- the set of approximation points p^{il} described in the following form: $(\tau_1^{i1}, \tau_2^{i1}, \tau_3^{i1})$, $\{[\tau_1^{il}, \tau_2^{il}, \tau_3^{il}]\}_{l=1,...L^1}$, where $(\tau_1^{i1}, \tau_2^{i1}, \tau_3^{i1})$ is its first point $p^{i1}, [\tau_1^{il}, \tau_2^{il}, \tau_3^{il}]$ is the vector used to generate the next its approximation points,
- the ξ_i value representing the half of thickness of the *i*-th localization snake came into being by fuzziness of the *i*-th curve taking into account element tolerances.

Finally, the fault dictionary has the form: $D_{IL} = \{(\tau_1^{nom}, \tau_2^{nom}, \tau_3^{nom}), \tau_{\mathcal{E}}, \{(\tau_1^{i1}, \tau_2^{i1}, \tau_3^{i1}), \{[\tau_1^{il}, \tau_2^{il}, \tau_3^{il}]\}_{l=1,..,L-1}, \}$

 $\xi_{i}\}_{i=1,..,I}$. It is placed in the program memory of the microcontroller. For *K*=3, *I*=5, *J*=32 (*J*=64) it consists of 499 (979) elements. Thus it is small in relation to the size of the program memory of typical 8-bit microcontrollers [14].

4. SELF-TESTING PROCEDURES

The self-testing procedure of the analog part is realized by the microcontroller controlling the embedded system and by its internal devices. First, the microcontroller executes the measurement procedure according to the measurement function (its algorithm is shown in Fig. 10), where the microcontroller generates the stimulant impulse with the duration time T determined by Timer 2, and it measures the duration times of the first three pulses of the response at the output of the analog comparator using Timer 1.



Fig. 10. The algorithm of the measurement function.

This procedure is realized in the main function, where a microcontroller initiates and activates its timers, introduces the tested circuit to an initial state, and starts square impulse generation by Timer 2 and the duration times counting by Timer 1, and next waits for the end of measurements of three duration times of the tested circuit time response. The services of timers are included in the Timer 2 Output Compare Interrupt Service, where only the Timer 2 is stopped, and the Timer 1 Input Capture Interrupt Service, where is changed the type of the active edge triggering this interrupt service and calculated time between rising and falling edges of a single impulse (the impulse duration time τ_k^{meas}).

Next, the microcontroller runs the detection procedure basing on the fault dictionary D_{IL} created during the design of the embedded system and the measurement result in the form of the measurement point p^{meas} with coordinates $(\tau_1^{meas}, \tau_2^{meas}, \tau_3^{meas})$ and, if a fault is detected, the localization procedure. The detection procedure bases on testing of the inequity:

$$\left\|\left\{\left(\tau_{k}^{meas}-\tau_{k}^{nom}\right)\right\}_{k=1,\dots,K}\right\|\leq\tau_{\varepsilon}$$
(10)

If it is fulfilled the tested circuit is fault free.

To localize a fault, we can use the localization procedure proposed in [13]. In this case we test if the measurement point p^{meas} is contained in the *i*-th localization snake. Generally, it is made by calculation of the minimum distance d_{min}^{i} between the measurement point and the set of the *i*-th curve approximation points $\{p^{il}\}_{l=1,..,L}$, and testing that d_{min}^{i} is smaller than the ξ_{i} . If it is fulfilled the *i*-th element is treated as faulty and it is added to the faulty element cluster. This cluster can contain only one element. In this case we have the unambiguous localization result. Obviously, it can contain more elements creating an ambiguous group of elements. This situation takes place when the measurement point is inside the area where two or more localization snakes penetrate themselves. Thus, each of these elements for which these snakes were created can be potentially faulty. If the tested circuit is faulty and this cluster after the localization procedure finish is still empty, it points that there are multiple faults in the tested circuit.

5. CONCLUSIONS

The author's significant contribution is the proposal of a new fault diagnosis method of soft single faults of passive components of analog circuits. The method was designed for BISTs used for self-testing of analog circuits (especially for aliasing filters of ADCs). For this method the new way of creation of the fault dictionary data for the fault detection procedure and the new measurement procedure controlled the BIST were elaborated.

The main advantage of this approach is the fact that it considerably simplifies the construction of these BISTs, and additionally the measurement procedure and diagnosis procedures are simple, that is their codes and the fault dictionary code do not occupy much space in the program memory of the control unit of the embedded system and these procedures need no big computing power. Thus, the proposed approach of self-testing of analog parts of embedded systems can be implemented with success in systems with control units with moderate computing power, e.g. in still popular and inexpensive 8-bit microcontrollers.

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