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PRECISE PHASE-SENSITIVE DETECTOR WITH SWITCHED TWO-TERMINAL RC NETWORK

Andrzej Met [1], *Krzysztof Musioł* [2], *Tadeusz Skubis* [3]

Institute of Measurement, Electronics and Automatic Control, Silesian Technical University, Gliwice, Poland
[1] email: andrzej.met@polsl.pl
[2] email: krzysztof.musiol@polsl.pl
[3] email: tadeusz.skubis@polsl.pl

Abstract - Application of a switched two-terminal RC networks for the construction of phase-sensitive detectors (PSDs) which are used in self-balancing transformer bridges is described. The switched two-terminal RC network makes possible effective reduction of noise level, increasing the CMRR, removing the input DC offset and providing the galvanic separation of the input and output circuits. Investigation of properties of the precise phase-sensitive detector used in a prototype self-balancing bridge for maintenance of inductance standard shows that the noise attenuation is bigger than 100 dB. Nowadays, the precise phase-sensitive detector described in the paper successfully operates in the automatic impedance bridge KWL[1] designed for high accurate inductance measurement at the Physikalisch-Technische Bundesanstalt in Braunschweig (PTB, Germany) [4].

Keywords: phase-sensitive detector, switched RC network.

1. INTRODUCTION

The accuracy of several important precise measuring instruments, typical of which are the automatic impedance bridge [3], and voltage or current comparator bridge [2], [4], depends particularly on the performance of the null detector used. Design engineers should remember that a very sensitive null detector doesn't guarantee reaching a high resolution of measurement. A main reasons of this are background noises and undesired interferences occurring on input of detector which effectively mask a usable signal. Taking the above under consideration, a key feature of the good null detector is its ability to detect a desired difference signal when high noise level occurs. The most common methods of reducing noise and interference in electronic circuits are filtering process and phase-sensitive detection [1]. Filters narrows the pass band to minimum eliminating thereby the noise of frequencies differing from the bandwidth. Unfortunately for changing the work frequency of measuring instrument is necessary to change the bandwidth of all bandpass filters using in its null detector circuit. A phase-sensitive detector, in turn, needs pre-amplification for unbalance signal level over ten milivolts. For lower signals accuracy of these detectors decrease rapidly. It is significant that noise and interference are amplified during the signal amplification. In case of high noise level to signal level ratio the amplifiers become saturated and then we can observe distortion of the original shape of the unbalance signal (Fig.1).

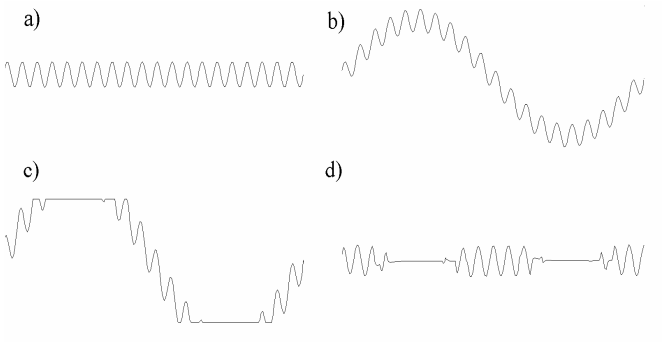

Fig.1. Distortion of unbalance signal caused by saturation of the amplifier: a) 1 kHz unbalance signal, b) unbalance signal with 50 Hz interference, c) distortion of the signal cased by saturation of the amplifier, d) distorted unbalance signal after filtration.

In order to reduce the deformation of the unbalance signal the null detectors are built as cascaded low-gain amplifiers interleaved with bandpass filters. However the filters cause angular change in the measurement signal. The shift is depended on accuracy of adjustment and stability of the electrical elements used. High phase shift occurs for filters which have a high quality factor. The phase shifts of all bandpass filters are added that leads to a wrong detection results for orthogonal components of unbalance signal.

The phase shifting issue is very important in a self-balancing devices. A significant phase shift in the amplification and filtering circuitry makes auto-balance process longer or can make the output signal unstable because of mutually interaction of orthogonal components.

Another important issue is the influence of the common-mode signal on the total unbalance voltage. Usually the unbalance signal provided to the null detector input consists of two voltages appearing across two separate pairs of input

[1] Polish abbreviation for Impedance Comparator Bridge

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terminals. Hence, a differential amplifier has to be used as the input stage of the null detector. A real differential amplifier also slightly amplify the common-mode signal which leads to a wrong measurement result of the unbalance voltage. A ratio of the differential signal gain to the common-mode signal gain is determined by the Common-Mode Rejection Radio (CMRR). In practice, the value of the CMRR depends on the accuracy and stability of the resistors used in the feedback loop of the amplifier. For AC signals the parasitic parameters of the resistors used and the parasitic coupling effects should be taken into account. As known, for the most of measuring instruments the best solution is based on application of instrumentation amplifiers which are particularly suitable for use in test and measurement equipment. However, in high-precision instruments used e.g. for impedance standard comparison the null detector should meet the highest accuracy requirements. Then commercial instrumentation amplifiers which doesn't guarantee the CMRR higher than 100dB (1kHz) cannot be applied.

2. SWITCHED RC NETWORK

As noted in the earlier consideration the main engineering problems appearing during design of the precise null detector are removing noise and interference from the useful signal without significant phase distortion and ensuring possibly high CMRR. A null detector circuit proposed by the authors, based on switched RC network, meets all the above requirements.

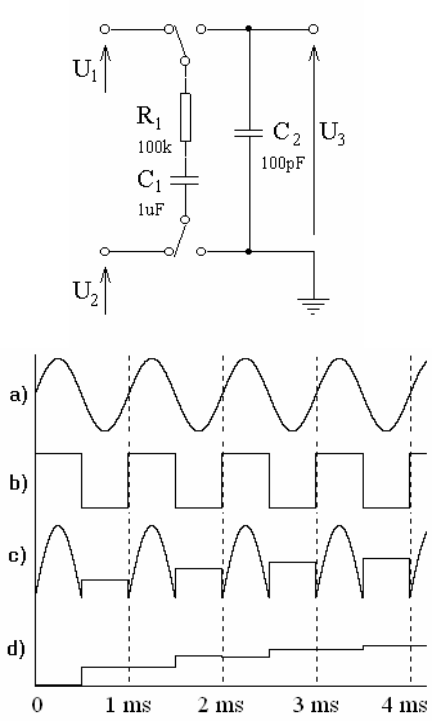

Fig. 2. Switched two-terminal RC network: a) differential signal U_1-U_2 , b) switching square wave, c) voltage on the RC network terminal, d) output signal U_3.

The circuit is equipped with a pair of CMOS switches which alternately connects a two-terminal RC network to an input voltage and after a half period (T/2) - across an output capacitor C_2 (Fig. 2). The 1 kHz switching frequency[2] is synchronous with the input sine wave frequency (Fig. 2a,b). If the two signals are in phase then the RC network is connected to the input voltage during positive values of the input sine wave. The situation is analogous to connecting the full-wave rectified sine to the two-terminal RC network. The capacitor C_1 is periodically charged until the voltage between its plates reaches the mean value of full-wave rectified sine, which equals

$$U_{\mathrm{AVG}} = \frac{2}{T}\int_0^{T/2}[U_1(t) - U_2(t)]dt = \frac{2}{\pi}\cdot U_m \qquad (1)$$

When the negative values of the input sinusoid wave are generated, the RC network is connected to the output capacitor C_2. Then a part of charge stored on the capacitor C_1 is transmitted to capacitor C_2. Because the capacitance of C_2 is much smaller then C_1 so the voltage across the capacitor C_1 decreases slightly. In a steady-state the voltages across C_1 and C_2 are equal and the charge doesn't flow. The capacitor C_2 acts in the circuit as an holding capacitor and can be loaded only by a high resistance input circuit like a voltage follower with FETs input.

As mentioned before, when the positive values of the switching signal are generated, the input differential voltage (U_1-U_2) is connected to the RC network. The common-mode signal doesn't have any influence on the charging process of the capacitor C_1. Theoretically the circuit shown in Fig.2 is characterized by an infinitely large CMRR. In practice, the parasitic capacitances of the switches limit the CMRR to about 120 dB. However, this value is high enough that the two-terminal RC network can be used in high-precision measuring instruments. The CMRR can be additionally increased by increasing the capacitance C_1 or by accurate equalization of the parasitic capacitances of the switches.
An additional advantage of the switched RC network use is galvanic separation between the null detector and the measuring circuit.

The two-terminal RC network has also high frequency-filtering properties. Impulse noises have a very small influence on charging process because of long time constant of the RC network. Other noises appearing on the input are averaged. The influence of the noises and interferences will be analyzed in the frequency domain. In Fig. 3a the spectrum W_1 of the sine wave input voltage affected by white noise U_{noise} is shown. The spectrum W_2 of the switching waveform is illustrated in Fig. 3b. When the value of the square wave is "1" the RC network is connected to the input voltage, whereas, when the level is "0" the RC network is connected to the output capacitor C_2. Because the mean DC voltage of such square wave equals 0.5 the spectrum has a peak in zero frequency. Voltage on the RC network terminal can be calculated in time domain as the

[2] In the KWL bridge the switching frequency equal to unbalance signal frequency is 1 kHz because of working frequency of the instrument. At National Measurement Institutes comparisons of inductance standards are usually carry out at 1 kHz.

product of the sine wave input signal and the square wave switching signal. Since multiplication in time domain corresponds to convolution in frequency domain we find that in frequency domain the signal on the two-terminal RC network looks like shown in Fig. 3c. According to the definition of convolution all harmonics of the square wave were shifted by the frequency f_s of the input signal. The frequency f_s component corresponds to a convolution of the fundamental frequency f_s component of the input sine wave and the DC component of the switching waveform. Since the switching frequency is synchronized with the input voltage frequency ($f_s = f_{sw}$), as the result of the convolution the first harmonic of the square wave was shifted to the zero frequency (DC).

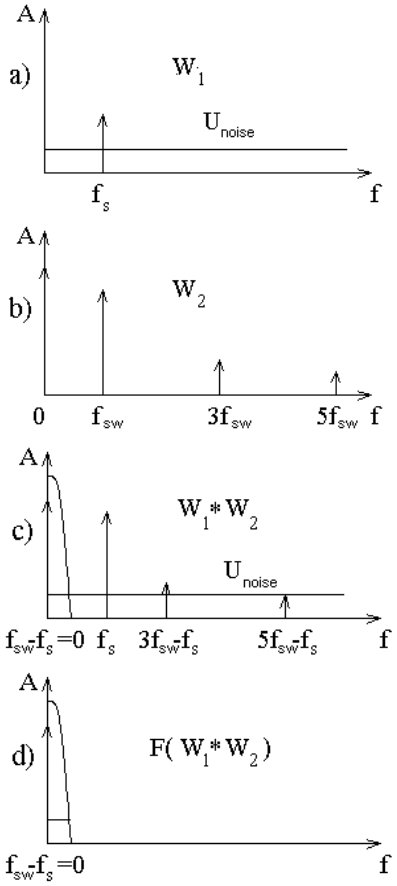

Fig. 3. Spectrums of signals: a) input signal with a noise, b) spectrum of switching square wave, c) signal on the RC network terminal (convolution of the spectrums W_1 and W_2), d) spectrum of the output voltage U_3.

The two-terminal R_1C_1 network acts also as the first-order low-pass filter. The cutoff frequency of the filter is determined by its R_1C_1 time constant. Taking all of the above under consideration, the higher harmonics content of the output voltage U_3 is reduced. The filter passes only very low frequency components. The components are generated mainly by noise sources around the fundamental switching frequency (influence of noise sources around the higher switching frequency is limited). For example, for component values refer to the Fig.2 the cutoff frequency equals 1.6 Hz, so the filtering efficiency is very high.

A main disadvantage of the circuit shown in Fig. 2 is that it passes the DC component to the output terminal. Theoretically, for a AC measuring instrument based on a transformer bridge it doesn't affect the measurement. However, for a high-precision instrument even voltage of the order of several μV generated in the measurement circuit according to the Seebeck effect may affect the right output unbalance signal. The other disadvantage is that the DC voltage is the usable output signal. The voltage should be significantly amplified. Then the input offset voltages and bias currents of the instrumentation amplifiers can distort the unbalance signal. Hence, the switched two-terminal RC network should operate with the op-amps which have the best DC performance.

3. DUAL SWITCHED RC NETWORK

The disadvantages mentioned above can be eliminated by modification of the circuit. In Fig. 4 a modified circuit consisting of two switched RC networks is shown.

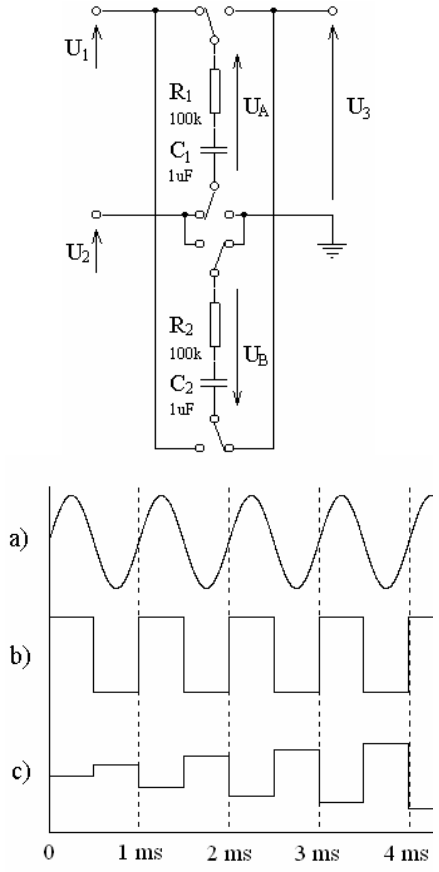

Fig.4. Alternately switched two-terminal RC networks: a) differential voltage U_1-U_2 , b) switching waveform, c) output signal U_3.

The structure and properties of each single network are the same as described in chapter 2. The inputs and the outputs of the networks are connected in parallel and the time constants R_1C_1 and R_2C_2 are equal. The principle of operation of the dual RC network is based on alternately

switching of two RC networks. If the first network is connected to the input voltage, then the second one is connected to the output terminal, and vice-versa. Because on the R_2C_2 network the negative part of the input sine wave appears, the voltage U_B has the same magnitude as U_A, but opposite sign. Hence, the output voltage U_3, being the sum of the U_A and the U_B (Fig. 4c), in the steady-state becomes the square wave with levels: +/- U_{AVG} (given by (1)). The frequency of the output signal is equal to the switching frequency and the frequency of the input sine wave. An essential feature to notice is that if a DC component appears on the input, it will be transferred to the output but the peak-to-peak amplitude of the output square wave is independent of the DC component and still equal to $2U_{AVG}$. The output signal U_3 is further amplified by the AC amplifier. However, the DC component transferred to the output isn't amplified by the AC amplifier. The input offset voltages of the operational amplifiers also don't affect the unbalance voltage. Additional advantage of the dual switched network is that the output square wave amplitude is twice the amplitude of the output signal for the single RC network.

The amplified AC signal is proportional to the component of the input signal which is in phase with the switching signal. The peak-to-peak value of the output square wave can be expressed as

$$U_{pp} = \left| 2 \cdot k \cdot U_{\mathrm{AVG}} \cos \varphi_{s,sw} \right|, \tag{2}$$

where: k – gain of the AC amplifier,
U_{AVG} – average value of the full-wave rectified input sine wave,
$\varphi_{s,sw}$ – angle between sine and switching waveforms.

The output square wave after amplification can be detected by the normal or the phase-sensitive detector. The following equation describes the mean PSD output voltage

$$U_{out} = \left| k \cdot U_{\mathrm{AVG}} \cos \varphi_{s,sw} \right|, \tag{3}$$

for the normal half-wave detector, and

$$U_{out} = k \cdot U_{\mathrm{AVG}} \cos \varphi_{s,sw}, \tag{4}$$

for the phase-sensitive half-wave detector.

The equation (4) shows that the phase-sensitive detection gives information about the amplitude and the phase difference of the input sine excitation and reference switching waveform.

4. PRECISE PHASE-SENSITIVE DETECTOR

A block diagram of the precise phase-sensitive detector using the dual switched two-terminal RC network is shown in Fig. 5. The first block is the dual switched RC network shown in Fig. 4. The output voltage U_3 is amplified by the AC amplifier with high gain. Because the RC network eliminates noises and interferences from the input sine wave, distortion of the original shape of the unbalance signal caused by the saturation of the amplifier (Fig. 1)

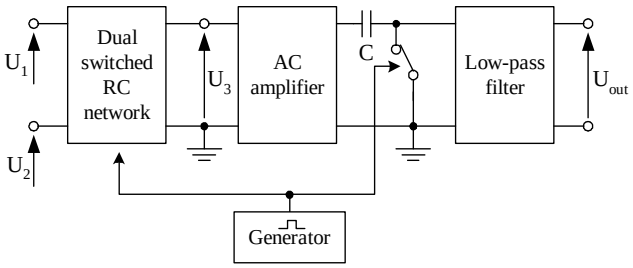

Fig.5. Block diagram of precise phase-sensitive detector using dual switched two-terminal RC networks.

doesn't occur. As a phase-sensitive detector acts an electronic switch which periodically grounds one plate of the capacitor C. On the output of the phase-sensitive detector the square wave with 50% duty cycle and the amplitude given by the (2) appears. The low-pass filter eliminates the switching frequency component and passes the usable DC component. The detector shown in Fig. 5 is a very high sensitive and noise-proof. Hence, it can be successfully used as a null detector in precise measuring instruments. Because of using the amplifier with high gain and the electronic switch with non-zero resistance, the gain of the unbalance voltage is not known precisely. This issue isn't important in null detector design but can be significant for phase-sensitive voltmeters design where it causes a small multiplicative error.

4.1. Feedback loop

A high stability of the gain of the unbalance voltage can be obtained by using the global feedback loop. In Fig. 6 a block diagram of a precise phase-sensitive detector with global feedback loop is shown.

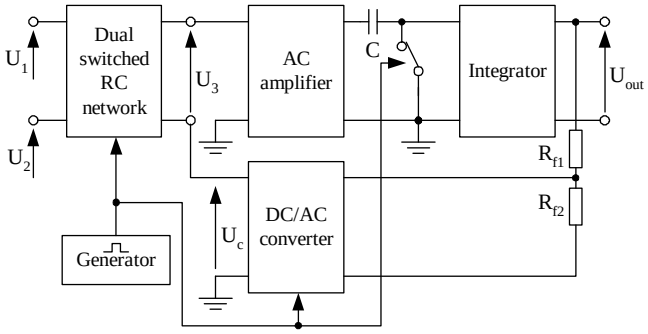

Fig.6. Block diagram of precise PSD with global feedback loop.

In the circuit the voltage from output of the phase-sensitive detector is delivered to the integrator. The mean DC voltage is returned from the output of the integrator through the resistive divider and the DC/AD converter to the input of the AC amplifier. The use of the feedback loop allows to set the DC voltage on the output of the integrator on the level for which the voltage on the input of the integrator equals zero (then $U_c = U_3$). The gain of the circuit is set by the precise resistive divider, consisting of two resistors R_{f1} and R_{f2}. When the input differential voltage is a

sine wave, the DC voltage on the output of integrator can be calculated using the following formula

$$U_{\text{out}} = \left(1 + \frac{R_{f1}}{R_{f2}}\right) U_{\text{AVG}} \cos\varphi_{s,sw} = \left(1 + \frac{R_{f1}}{R_{f2}}\right) \frac{2U_m}{\pi} \cos\varphi_{s,sw} \cdot \quad (5)$$

The DC/AC converter can be performed with the use of the electronic switch or the switched holding capacitors (in a circuit similar to that shown in Fig.4). The RC network, the phase-sensitive detector and the DC/AC converter have to be switched synchronously. Hence, the three components are controlled by the same square wave generator with the phase and frequency depended on the input signal. The time needed to achieve steady-state is depended on the RC network time constant and the integration time constant.

5. INVESTIGATION OF PROPERTIES OF THE PRECISE PHASE-SENSITIVE DETECTOR

Noise influence on the output signal of the phase-sensitive detector was investigated in the measurement circuit shown in Fig. 7.

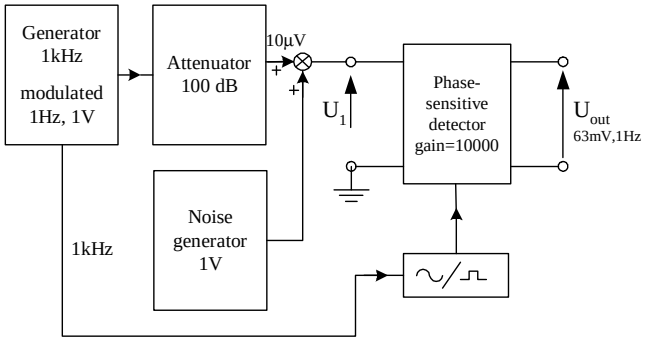

Fig. 7. Measurement circuit for the investigation of properties of the phase-sensitive detector.

The 1 kHz sine wave signal amplitude-modulated by the 1 Hz sine wave was delivered to the input of the precise phase-sensitive detector through the resistive divider.

Because of modulation the maximum voltage on the output of the generator was changing from 1 V to zero. The resistive divider with a ratio of 100 000:1 (100 dB) consisting of 1 MΩ and 10 Ω resistors reduces the maximum voltage to 10 μV. The gain of the phase-sensitive detector was set to 10 000 using the resistive divider R_{f1}, R_{f2}. The voltage on the output of phase-sensitive detector was displayed on a digital oscilloscope. The DC offset of the output voltage was waving between 0 and 63 mV with frequency 1 Hz. Thereafter a white noise (bandwidth 0-100 kHz, U_{rms} = 1V) was added to the usable signal. The output voltage observed on the oscilloscope was distorted by the noise, but its amplitude was so small that the 1 Hz sine wave signal was well visible. According to predictions it was noticed that the output noise contains mainly low-frequency components. Since the noise voltage added on the input of the phase-sensitive detector was 100 000 times bigger than the input signal voltage, and on the output of the detector it was smaller than the usable signal, we can conclude that the noise attenuation is bigger than 100 dB.

6. CONCLUSIONS

The phase-sensitive detector operating particularly as a synchronous rectifier has an important role in many benchtop instruments. The performance of the PSD determines the accuracy and frequency range of the overall instrument. The described precise phase-sensitive detector equipped on the input with the dual switched RC network has many advantages which make it suitable for use in high--precision measuring instruments, especially in self-balancing transformer bridges. The main advantages of the detector are the very high noise attenuation (bigger than 100 dB), the high CMRR (about 120 dB) and elimination of the input DC offset. Additional advantages are the total galvanic separation of the input and output circuits and the very small phase error (less than 0.1 degree) because of lack of tuned band-pass filters.

The dual precision switched capacitor instrumentation building block LTC1043 was used as the switched RC network. It ensures precise, charge-balanced switching and operates up to 5 MHz clock rate [5].

Further investigation will be performed to determine the frequency characteristic of the noise attenuation. Theoretically, we can predict that the bigger distortion of the output signal will be caused by the noise sources around the fundamental frequency of the input sine wave (see Fig. 3).

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