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# VIRTUAL TESTING METHOD FOR STATIC ADC NON-LINEARITY – RSD CYCLIC A/D CONVERTER CASE

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**Abstract** – One of the recent approaches to test A/D converter performance is the so-called Servo-Loop Method. This method is aimed at the non-linearity extraction of static ADC transfer curve. In this paper, we prove an advanced Servo-Loop version focusing on behavioral and transistor-level example of the Residual Signed Digit (RSD) cyclic A/D converter design. The background of the considered Servo-Loop version was proposed in [1]. In this paper, we establish a Virtual Testing Environment (VTE) built on Verilog-A implementation of the Servo-Loop unit fully integrated into Cadence design environment. Powerful capabilities of the proposed VTE were successfully confirmed by a large set of behavioral and transistor-level simulations in Spectre.

**Keywords**: A/D Converter testing, Servo-Loop method, Cyclic RSD A/D converter.

## 1. INTRODUCTION

Extraction of design performance is a challenging task in A/D Converter testing. This is backgrounded by the fact that the ADC performance expressed in terms of *integral* and *differential* non-linearity (*INL* and *DNL*) depends on many parameters present in the analog design part. Moreover, in high-resolution ADC devices it is often not feasible to extract their total response because of the large number of digital states. According to the test setup, the existing performance extraction methods can be classified into *open-loop* or *closed-loop* category [2]. The *code-density* method [3], [4] is a typical representative of the open-loop category, producing an estimation of the code transition levels from the histogram of a large set of recorded ADC device characteristics. In our work, we focused on the performance extraction based on full transistor-level simulation of the ADC integrated circuit design; at this point, any statistical processing (e.g. histogramming) is not acceptable because of the unsuitably long simulation time. Therefore, an iterative algorithm to find the code transition levels, based on a single ADC response capture is highly recommended. The *Servo-Loop*, belonging to the closed-loop extraction methods is the primary candidate to perform this task. The main principle of a standard Servo-Loop implementation [4] is that a feedback loop is accomplished across the ADC under test,

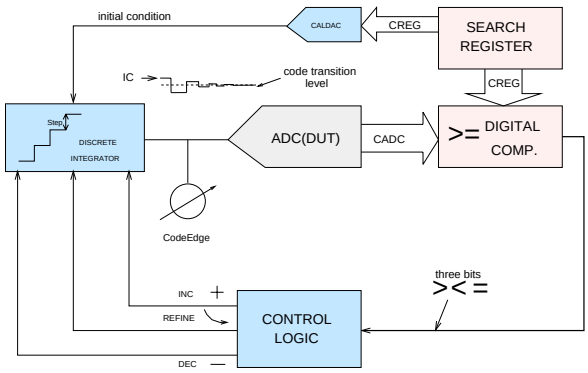


Fig. 1. Proposed Servo-Loop implementation.

*analog integrator* and digital comparator blocks. Subsequently, the algorithm searches for the code transition level of a given code, performing a conventional *linear search*.

The Servo-Loop method is widely used for direct A/D converter test and measurement. However, to implement this method in a simulation way into advanced IC design tools, improvements of the standard implementation are strongly advised as to increase the performance and efficiency of the search algorithm. We successfully made such improvements in [1], significantly accelerating the Servo-Loop convergence. The subsequent task being the main topic of this paper is to develop a Virtual Testing Environment (VTE). The VTE proposed incorporates the Servo-Loop core and creates a convenient user interface for IC design engineers involved in the A/D converter design and verification. Particularly, the VTE is dedicated to solve the following tasks. First, it is capable to simulate a behavioral ADC model annotated by a priori known circuit error sources and to extract INL and DNL performances invoked by these errors. The individual error source contributions to the total ADC performance can be then evaluated. In such a way, the most crucial parameters for a given ADC circuit implementation are pinpointed, enabling a system-level design optimization. Secondly, the VTE enables to run full transistor-level simulation necessary for the verifications carried out in the IC design practice. At this point, the accelerated Servo-Loop convergence offers a significant advantage during the IC verification process.

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In Section 2, the main advantages of the considered powerful Servo-Loop implementation are summarized. In Section 3, Virtual Testing Environment idea is presented, describing the Verilog-A system background for use with Cadence design environment, particularly the Spectre circuit simulator. In Section 4, we demonstrate the system architecture and behavioral model of the RSD A/D converter used as a Device Under Test (DUT) for the proposed VTE. Section 5 deals with the most important verification results of the ADC design prototype, discussing various models from fully behavioral to advanced circuit-similar level. Finally, in Section 6, the work conclusions are stated.

## 2. ADVANCED SERVO-LOOP IMPLEMENTATION

In this Section, we comment the background for a powerful extension of the conventional Servo-Loop algorithm to accelerate its convergence speed and reduce the total extraction time. In Fig. 1, the proposed implementation of the Servo-Loop algorithm is shown, which is generally usable for simulation-based extraction of ADC INL and DNL. In comparison with the standard implementation [5], the following innovations were suggested.

- **Discrete integrator applies a priori known step values to the ADC input signal.** From these values, the corresponding transition levels can be directly established (with no necessity to check or measure what the ADC input signal is).
- **Convergence process is significantly accelerated** for two reasons. First, an initial condition has been applied to the ADC input, based on the estimation provided by CALDAC block. During the first iteration cycle, the difference between the $C_{ADC}$ and $C_{REG}$ codes is therefore reduced, speeding up the feedback search for an equilibrium point. A small initial step of the integrator output can be therefore chosen, typically less than 1 LSB. The second reason of the convergence speed-up arises from the fact that the integrator step value is being continuously refined during the iteration process by the *damping factor* of $\varepsilon<1$.

To demonstrate the performance of the novel Servo-Loop implementation, a comparison against conventional linear search method is shown in Table 1. Note that the symbol *[]* denotes the integer-round operator. The standard implementation (cf. linear search in the second column) exhibits inversely-proportional dependence of the accuracy $\Delta_{LSB}$ versus number of iteration cycles denoted here as $N_{cycle}$. Thus, while requiring high levels of accuracy, the application of the standard variant takes unacceptably long, expressed in term of iteration cycles. In our Servo-Loop variant (see the third column), the number of cycles required for a given accuracy follows a logarithmic trend. Consequently, this results in significant time savings while applying the proposed method in high performance circuit simulation.

Table 1 Performance comparison expressed in number of iteration cycles(for $\varepsilon=2/3$).

| Accuracy $\Delta_{LSB}$ | Linear search $N_{cycle}=[1/\Delta_{LSB}]$ | Proposed method $N_{cycle}=[1+\log(\Delta_{LSB})/\log(\varepsilon)]$ |
|---|---|---|
| 100 mLSB | 10 | 7 |
| 10 mLSB | 100 | 12 |
| 1 mLSB | 1000 | 18 |

## 3. PROPOSED VIRTUAL TESTING ENVIRONMENT

In this Section, the implementation of the Servo-loop unit (further denoted to as *Servo-Looper*) from Fig. 1 into Cadence design environment is presented as well as possibilities and advantages of the VTE.

The Servo-Looper was designed using Verilog-A in the form of a behavioral model. This implementation makes the Spectre simulations of the VTE shorter and the changes in the Servo-Looper easier to implement. The Servo-Looper features are as follows.

- It is able to work with ADCs with resolution of up to 15 bits.
- Parameters of the Servo-Looper model are number of iteration cycles, iteration parameter ε, range of testing and the sweep of the testing.
- Generates output text files containing INL and DNL for each code, gain and offset error and also code-edge values of every code of the tested ADC.
- It maintains full compatibility with the Cadence simulation environment; waves of the INL and DNL are can be easily opened by the Wavescan viewer.

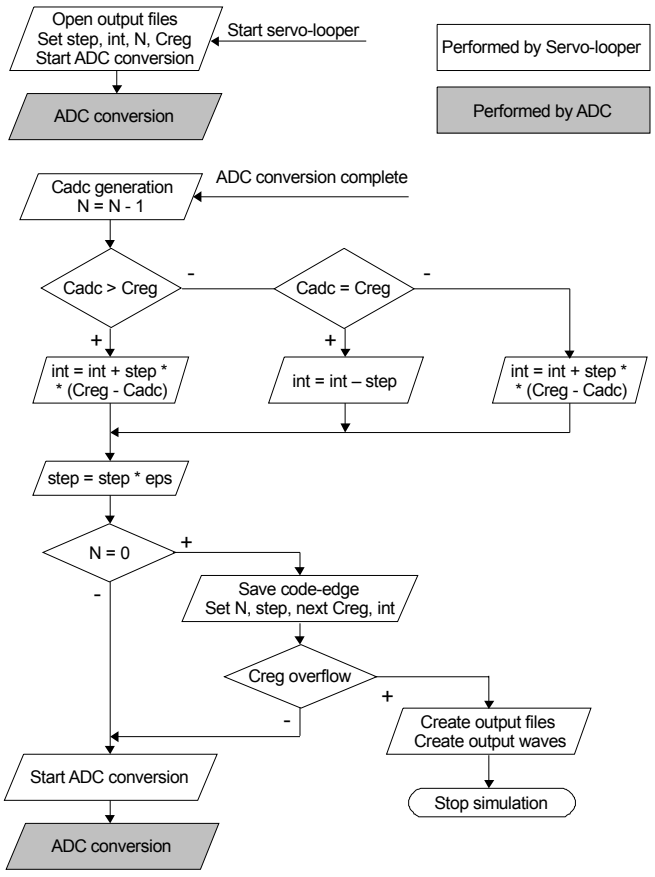

Fig. 2 Flowchart of the Servo-Looper.

The flowchart of the Servo-Looper applied in the proposed VTE is shown in Fig. 2. Here, the *step* variable denotes the difference of the input signal in two different iteration cycles, *int* is input signal of the tested ADC forced by the Servo-Looper, *N* is number of iterations left, *ε (eps)* is the iteration parameter, *Creg* is the code of the tested input value and finally, *Cadc* is the binary representation of the ADC output, further denoted to as *output code*.

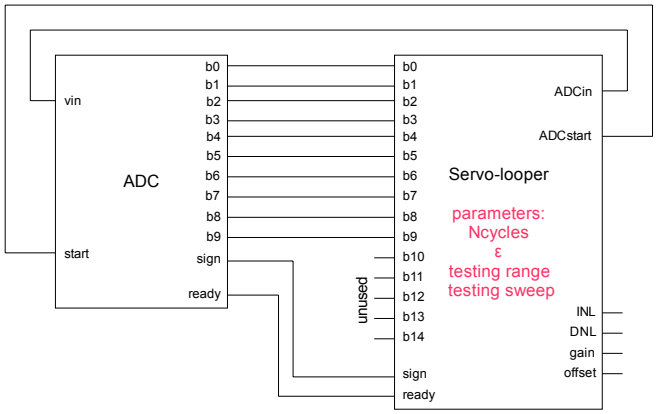


Fig. 3. VTE schematic.

The simplified schematic of the VTE is shown in Fig. 3. The Servo-Looper forces input signal to the ADC by the pin *ADCin* and starts the ADC conversion by the signal from pin ADCstart. The end of the A/D conversion is indicated by the signal *ready*. The speed of the simulation is affected mainly by the A/D converter as a matter of fact that the Servo-Looper is effectively implemented in Verilog-A with no additional delays in timing. The voltages of the nets *INL*, *DNL*, *offset* and *gain* are proportional to the appropriate metrics of the ADC.

## 4. CYCLIC RSD A/D CONVERTER

In this Section, the introduction to the cyclic RSD A/D converter, its model and verification methodology is presented.

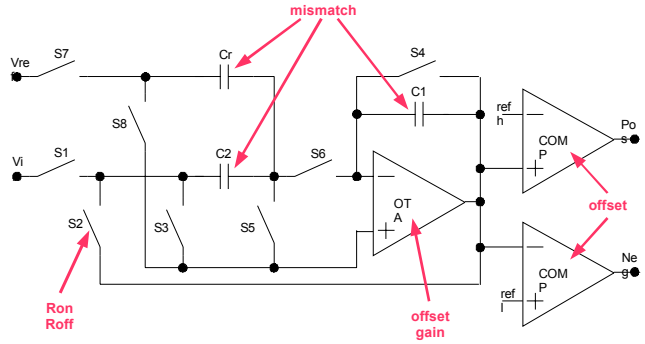


Fig. 4. Analog ADC core and its non-idealities.

We created a hierarchical model of the presented ADC in Verilog-A. The analog core is shown in Fig. 4. The crucial ADC elements C1, C2 and Cr together with the OTA perform the multiply-by-two and subtraction operation, conditioned by the switches from Vi or Vref voltage source. Two comparators connected to the OTA output generate bipolar RSD code for every converted bit. A detailed functional description of the considered ADC can be found e.g. in [6]. The purpose of the ADC model creation is to have a quick evaluation of its function, i.e. fast and effective verification of the transfer characteristic for Verilog-A models using Servo-Looper. Additionally, we also obtain the ADC sensitivity characteristics, i.e. the influence of the non-ideal components of the analog core to INL, DNL, offset and gain errors. The sensitivity analysis is of an utmost importance so as to create the design specification for the critical ADC components.

The main non-idealities of the analog devices invoking error mechanisms in the considered ADC (see Fig. 4) are: input voltage offset and finite voltage gain of the operational amplifier, Ron and Roff of the switches, mismatch of the capacitors and input voltage offset of the output comparators.

To gain credible results from the sensitivity analysis on a particular error mechanism, it is necessary to keep all other errors present in the Verilog-A ADC model as close as possible to zero. However, one can meet with convergence difficulties in such idealized model; at this point, the switch or operational amplifier model can cause particular difficulties. To prevent this issue, several levels of the crucial component models were created. For instance, our switch model offers three levels varying upon the switch resistance with respect to the control voltage. These are the basic models providing Ron and Roff resistance values, linear model and exponential model. The best results were proven by the exponential model. The operational amplifier model must have finite voltage gain and finite gain bandwidth so as to protect from numerical instability which can occur by switching its input. More details of the actual model tuning will be presented in the full paper.

## 5. VTE VERIFICATION RESULTS

In this Section, the results of the VTE verification using test-bench from Fig. 3 supplemented by the RSD ADC model from Fig. 4 are presented.

Verification of error generating mechanisms mentioned in Section 4 was performed. First simulations were carried out for a low number N of iteration cycles so as to find out the influence of the ADC transfer curve on each non-ideality of the circuit.

The INL results for various values of operational amplifier input voltage offset are shown in Fig. 5. Here, the INL characteristic is evaluated for two OTA offset error values, 5mV and 10mV. As it can be observed in the simulated curves, the INL magnitude is linearly proportional to the offset error value. In a wider context, this underlies the linear superposition principle valid for the model-based testing under restrictive conditions given in [4].

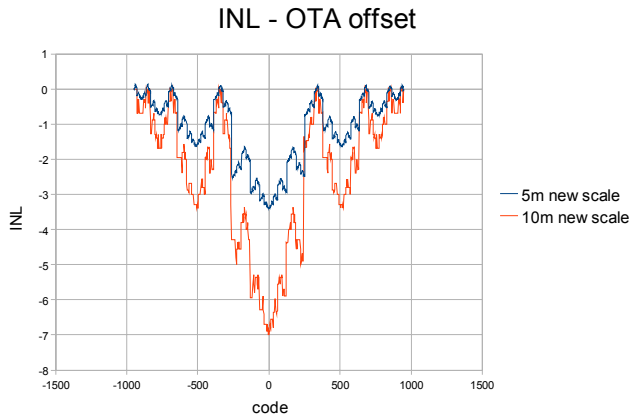


Fig. 5 Verification for various offset values.

Afterwards, more precise simulations were performed for the specified values of the analog components. An example of various precision level applied to the verification process is documented in Fig. 6. It represents INL for capacitor mismatch between C1 and C2 (see Fig. 4) for 5 and 10 iteration cycles, respectively.

Other results are presented in Fig. 7 and Fig. 8, documenting the remaining sensitivity characteristics of the ADC model.

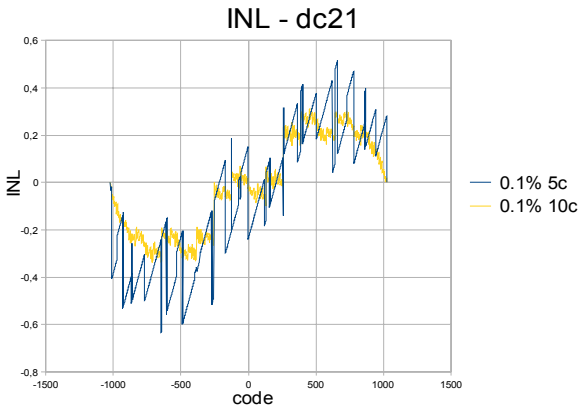


Fig. 6 Verification for various Ncycles.

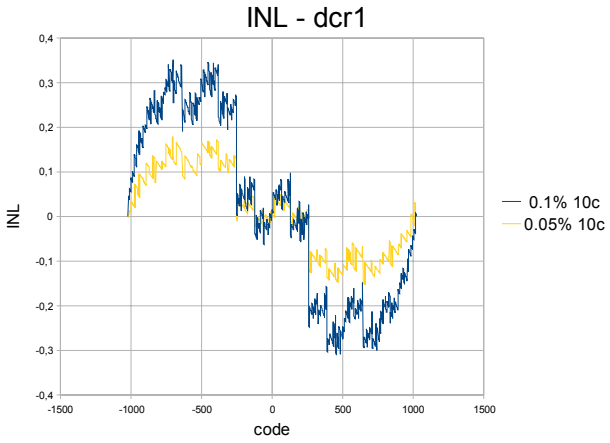


Fig. 7. Verification of Cr and C1 mismatch.

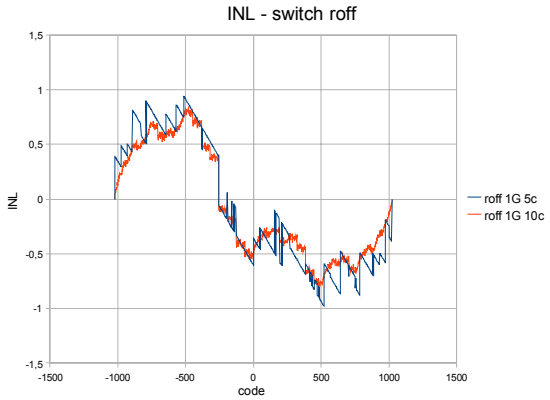


Fig. 8 Verification of switch Roff.

Finally, we attach the information about ADC simulation time.

- Complete Verilog model: 30 minutes
- Transistor level OTA: 3 hours
- Transistor level OTA and switches: 6 hours

## 4. CONCLUSIONS

The presented paper brings the most significant results of the ADC simulation procedure, including the description and setup of the testing environment. The VTE proposed is dedicated for the semiconductor industry practice and it already has been found as a useful tool for IC design engineers.

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