XIX IMEKO World Congress
Fundamental and Applied Metrology
September 6–11, 2009, Lisbon, Portugal

# ECONOMICAL TEST OF INTERNAL ADC IN EMBEDDED SYSTEMS

*Josef Vedral, Jakub Svatoš, Pavel Fexa*

CTU of Prague, Faculty of Electrical Engineering, Technicka 2, 166 27 Prague,
vedral@fel.cvut.cz, svatoj1@fel.cvut.cz, fexap1@fel.cvut.cz

**Abstract** – This paper describes two methods for economical test of dynamic parameters ADCs in embedded Data Acquisition Systems. First method is Exponential Fit Test, second method is Wobbler Test. Common testing methods are mentioned as far the accuracy and time necessary for the complete test are concerned. The tests for fast evaluation of the dependence of an effective number of bits on frequency of input signal are described and the comparison of proposed method with the standard methods is given.

**Keywords**: ADC test, Exponentional Fit Test, Frequency Wobbler test

## 1. INTRODUCTION

There are several common well-described indirect methods of ADC testing that are suitable for an evaluation of the reduction of the *Effective Number of Bits* (*ENOB*) on the frequency of input signal ([1], [2]). For example, the if one has 16-bits AD converter, it is necessary requires to take 64 kilo samples for 0,1LSB error of estimation of *ENOB* with *Sine Wave Fit Test* and equivalent number of samples for 0.1dB error of estimation of *Signal Noise and Distortion SINAD* with *Discrete Fourier Transform Test*. These series of samples must be taken for each frequency point individually.

Similarly to the previous case, the series of harmonic signals must be sampled. It is necessary to avoid leakage error by using coherent sampling.

## 2. EXPONENTIONAL FIT TEST

The *Exponentional Fit Test* is based on best fitting of exponential signal to the tested digitizer output signal. If samples are acquired from one period of output signal, it is possible to reconstruct the exponential signal by means of least-square fitting method

$$x_n = A e^{-Bt} + C \qquad (1)$$

where $A$ is the reconstructed signal amplitude, $1/B$ is its time constant and $C$ is its DC value. *RMS* error of this fit $\varepsilon$ denotes the tested digitizer *Average Effective Number of Bits* is defined

$$ENOB_{AVG} = n - log_2\left(\frac{\varepsilon}{RMS_q}\right) \qquad (2)$$

where $n$ is the nominal number of digitizer bits and $RMS_q = 2^{-n}/\sqrt{12}$ is the RMS value of its quantizing error.

The exponentional signal is easy generated out of rectangular signal by means of passive *RC* element filtration, where time constant $\tau = RC$, see Fig.1.

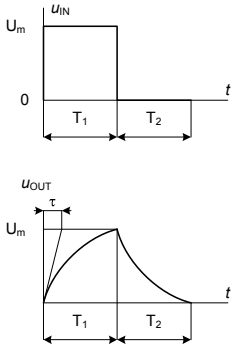


Fig. 1. Exponential signal generation.

Exponentional signal is defined as

$$U_C(t) = U_m\left(1 - e^{-\frac{t}{\tau}}\right) \qquad (3)$$

where $U_m$ is input rectangular signal amplitude.

To achieve the final output steady-state signal having the difference from theoretical value less than the resolution of the tested digitizer with nominally $n$ bits, the minimum ratio between $T_1$ ($T_2$) and time constant $\tau$ is given by

$$T_{1(2)} \geq \tau(n+1)ln2 \qquad (4)$$

For example, 16-bit digitizer requires the period of input rectangle $T \geq 11\tau$.

If the duty factor is $T_1 = T_2 = T$ the frequency spectra of both exponential curves are identical and given by expression

$$A(\omega) = \frac{1}{\sqrt{1+(\omega\tau)^2}} \qquad (5)$$

ISBN 978-963-88410-0-1 

For $\omega\tau >> 1$ is $A(\omega) = 1/\omega\tau$ and amplitude decreases with a slope – 20 dB/decade, see Fig. 2.

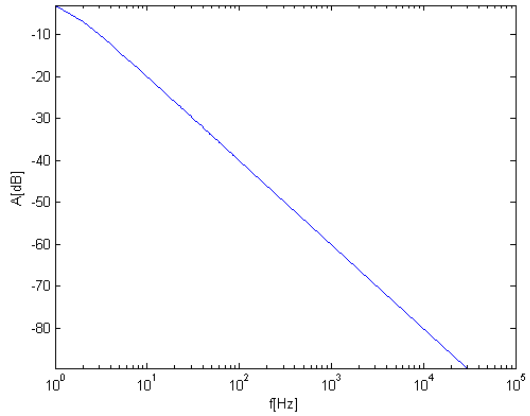


Fig. 2. Frequency spectra of exponentional signal.

## 3. FREQUENCY WOBBLER TEST

The basic idea is to apply the full-scale wobbler signal to the input of the tested ADC located on the chip of microprocessor. The frequency sweep of the wobbler signal should cover the desired range of dynamic test and the length of the wobbler depends on available memory space for the output series of samples as well as on desired accuracy of the test and on the availability of synchronisation of signal sampling. An estimation of the reduction of *ENOB* due to the increase of input signal frequency is calculated from measured series of samples. The Fig. 3 shows signal generated in ADC test.

The advantage is the reducing of acquisition time (to 50%) but more complicated arrangement and software are required.

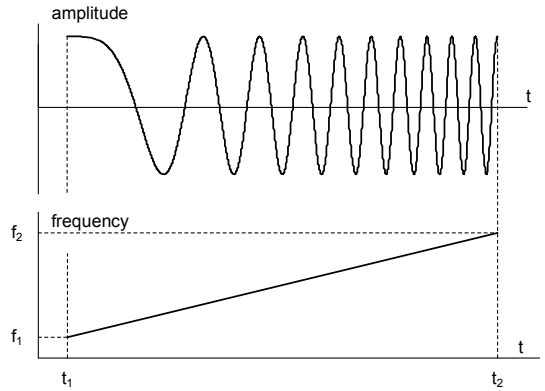


Fig. 3. Wobbler signals generated in ADC test.

## 4. DATA PROCESSING IN WOBBLER TEST

The first step of the algorithm is the rough analysis of sampled data. The measured data stream is divided into substreams. Each substream contains integer number (one or more to reach necessary number of samples for the next steps of algorithm) of quasi-periods of sampled chirp. These are tested for amplitude stability (using windowed *RMS* calculation).

The behaviour of input analog part of AD converter is estimated during this step. The input chirp can be described by the following formula¨

$$u(t) = A\sin\left[2\pi t\left(\frac{t-t_1}{\Delta t}(f_1 - f_2) + f_2\right) + \varphi\right] \quad (6)$$

where $A$ is the amplitude of the chirp, $t_0$ is the start time of chirp, $\Delta t$ is the duration of the chirp, $f_0$ is the start frequency of the chirp, $f_1$ is the stop frequency and $\varphi$ is the start phase of the chirp. In (1), linear frequency sweep is considered.

$$\frac{df}{dt} = \frac{f_1 - f_2}{\Delta t} \quad (7)$$

The least square algorithm is applied to each substream to fit ideal above described quasi-period (1) to the measured one.

To reduce the necessary time of solving the non linear system equation, not every parameters is optimised during the fitting. In the concrete case $f_0$, $f_1$ are the optimized parameters while other parameters are found by other ways before:

Parameter $t_0$ (start time of quasi-period defined as the zero crossing of measured signal) is calculated using linear interpolation from the two nearest (one negative and one positive) samples. In the case of noisy signal more complicated higher-order interpolation using more samples should be used. Parameter φ is automatically equal to zero when the above described definition of $t_0$ is considered.

Parameter $\Delta t$ (the duration of the current quasi-periods of the chirp) is calculated as the difference of the current $t_0$ and the value of $t_0$ of the next substream.

The effective value of the current quasiperiod - $A$ - is calculated using the following formula:

$$A_{est} = \sqrt{\frac{2}{\Delta t}\sum_{t_i} U^2(t_i)} \quad (8)$$

where $i$ includes all indices of samples taken between $t_0$ and $t_0+\Delta t$.

The last step of the algorithm is the calculation of the reduction of *ENOB* on the instant frequency of the input wobbler. The calculation of the *Average Effective Number of Bits* is done using formula

$$ENOB_{AVG} = \log_2 \frac{FS}{\sigma_f \sqrt{12}} \quad (9)$$

where $\sigma_f$ is the standard deviation obtained as a final result of chirp fitting of the substream in which

$$f = (f_1 + f_2)/2 \quad (10)$$

Minimum of $\sigma_f$ is the criterion of the best fitting by the least square method.

## 5. ACCURACY AND SPEED

Accuracy of the proposed method can be estimated by the comparison with the values of sine-fit test for 16-bit AD converter. The 256 samples must be taken to achieve 0,1 bit accuracy in *ENOB* estimation. If each substream contains more than 256 samples, one can say that the accuracy is equal or better than 0.1 bit (each substream is considered as a part of harmonic signal with frequency $(f_1+f_0)/2$). If 20 measured points are necessary to plot the graph showing the dependence of *ENOB* on the frequency, at least 5120 (=20x256) samples must be taken for such accuracy.

The superior chirp generator is required. Most of DDS-based generators are not suitable because the frequency sweep is synthesised from discrete frequency steps and these degrade the results of test.

The proposed test seems to be the fastest way of *ENOB* estimation. The speed of processing may be even enhanced by introducing the multiprocessor approach, see Fig 4.

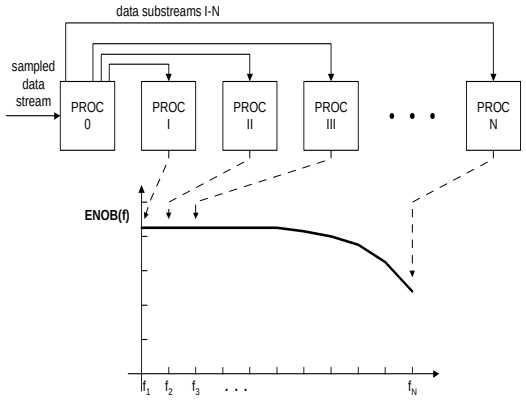


Fig. 4. Multiprocessor approach to test algorithm.

## 6. COMPARISON AND RESULTS

Each here described method has been implemented in FPGA Start Development Kit Cyclone II by Altera. Internal controlled DDS generator with 24 bit DA converter has been used to generate wobbler signal in frequency range from 20 Hz to 20 kHz.

The average *ENOB* = 13,9 bits by *Exponential Fit Test* and average *ENOB* = 14,1 bits by *Wobbler Test* in the frequency range up 20 Hz to 20 kHz is relevant to *ENOB* plot, determined by classical *Sine Wave Fit Test* method.

In Fig. 5 is presented *ENOB* plot for internal ADC converter by *Single Sine Wave Fit Test*. Average *ENOB* by this method is 14,2 bit. The average *ENOB* by this methods is 14,2 bits. The difference of 0,3 bit between *ENOB* and average *ENOB* is practically insignificant.

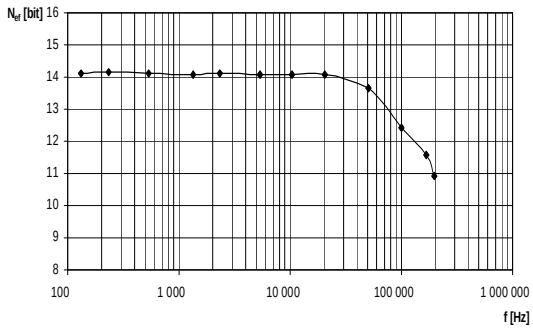


Fig. 5. ENOB plot for Single Sin Fit Test.

In Fig. 6, Fig. 7 and Fig. 8 is presented FFT plot of *Noise Histogram Test* with grounded input, *Code Words Histogram Test and FFT plot* of sinus signal 1 kHz.

The effective resolution of internal converters under test defined by formula

$$ER = \log_2 \frac{FS}{RMS_{NOISE}} \qquad (11)$$

is 15,4 bit. In FFT plot in Fig.6 are evident parasitic spectral components with USB supply noise under 100 dB.

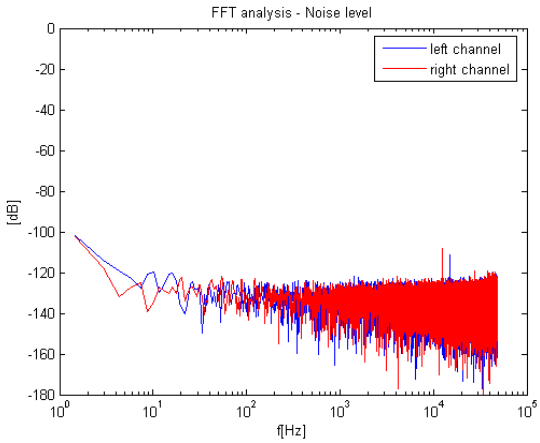


Fig. 6. FFT plot of Noise Histogram Test.

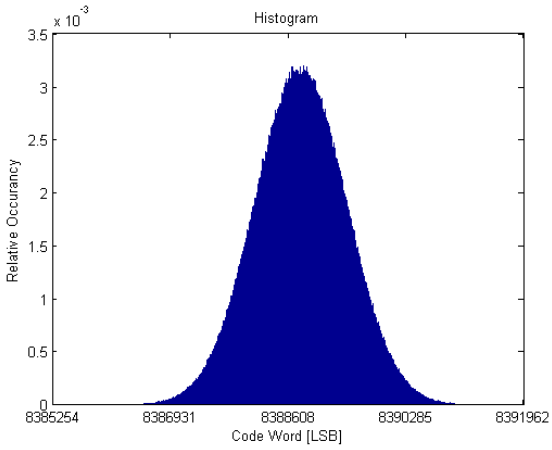


Fig. 7. Code Words Histogram Test.

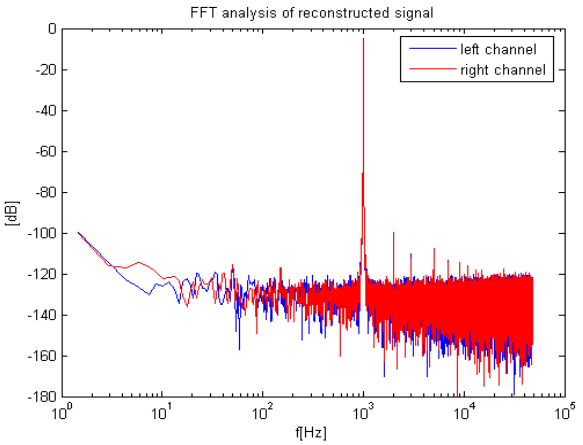


Fig. 8. FFT plot of sinus signal 1 kHz.

In Table I is comparison of results all tests applied in internal ADCs in FPGA Altera II.

From measured examples in Tab.I is evident very large reduction of number of samples in application of *Wobbler Test* and *Exponentionel Fit Test*.

From measured examples in Tab. I a very large reduction of number samples in application of the Wobbler and Exponentionel Test is evident. The reduction of samples is very significant for economical aspects of dynamic testing internal ADCs in Embedded Data Acquisition Systems.

Table 1. Comparison results of tests.

| Sine Wave Fit Test Discrete Fourier Transform Test | | | Wobbler Test | Exp Test |
|---|---|---|---|---|
| Freq. | 1 kHz | 10kHz | 20Hz – 20kHz | |
| *ENOB* | 14,7 bit | 13,8 bit | 14,1 dB | 13,9 dB |
| *SINAD* | 90,2 dB | 84,8 dB | | |
| *THD* | 103 dB | 95 dB | | |
| *SFDR* | 102 dB | 92 dB | | |
| *SNHR* | 94 dB | 86 dB | | |
| *ER* | 15,4 bit | | | |
| Number of samples | 64 k Frequency range 20Hz – 20kHz In 10 steps | | 5120 | 1024 |

The nominal parameters of tested audio codec Terratec 26 B is certificed: $THD \leq 105$ dB and $SINAD \geq 98$ dB from input sinus signal 1 kHz.

## 7. CONCLUSION

In the article is two high speed test methods proposed. Due to high speed of test, the above described method may be suitable when the necessity of testing of many pieces of ADCs is
required, e.g. at the end of manufacturing process.

## ACKNOWLEDGMENTS

This project is supported by the research program No. MSM6840770015 "Research of Methods and Systems for Measurement of Physical Quantities and Measured Data Processing" of the CTU in Prague sponsored by the Ministry of Education, Youth and Sports of the Czech Republic.

## REFERENCES

[1] IEEE Standard 1057-1994, “IEEE Standard for Digitizing Waveform Recorders".

[2] IEEE Standard 1241 - 2000, “IEEE Standard and Teminology and Test Methods for Analog-to-Digital Converters.

[3] Holub, J. - Šmíd, R. - Vedral, J.: Chirp Based Method for ADC Testing: Simulation and Evaluation. *IEE Conference* Advanced A/D and D/A Techniques and Their Applications. Glasgow: University of Strathclyde, 1999, p. 94-96.

[4] Holcer, R., Michaeli, L.: DNL ADC Testing by the exponential shaped voltage. *IEEE Transaction on Instrumentation and Measurement*, vol. 52, No. 3, (2003), p.946-9.

[5] Vedral, J., Neskudla, J.: Measurement of ADCs Effective Resolution. *IEE International Conference on Advanced A/D and D/A Conversion Techniques and thein Applications.* Limerick 2005, p. 255-257.

[6] Vedral, J.: Exponential Fit Test - Theoretical Analysis and Practically Implementation. *13th Workshop on ADC Modelling and Testing* [CD-ROM]. Florence: University of Florence, 2008, p. 1033-1036.

[7] Vedral, J.: Implementation of ADC Wobbler Test in FPGA. In *DCIS 2008 - Conference on Design of Circuits and Integrated Systems*. Grenoble: TIMA, 2008, CD ROM.

[8] Cyklone II FPGA Starter Development Kit, http://www.altera.com.