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A NOVEL APPROACH FOR TEACHING DIGITAL IMAGE PROCESSING BASED ON A NEW MULTI-SCALABLE HARDWARE PLATFORM

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Abstract - This paper highlights the capabilities and significance of a new multi-scalable hardware platform developed at image processing research group of the Ilmenau University of Technology. The main objective is a combination of theory and practice in the education of image processing. The use of image processing for measurement tasks becomes more frequently. The aspect like a camera works is taught, however frequently it cannot be practically experienced by the students. Due to the increasing miniaturization purchased cameras are not suitable for this object.

The hardware with the corresponding training modules presented in this paper give a novel approach to close this gap. Thru the modular structure, students are allowed to solve problems iterative.

Keywords: image processing, hardware platform, education

1. INTRODUCTION

Image processing technologies gain in importance in the industrial metrology. As manufactured components become smaller and tolerances tighter, more data points must be collected and analyzed to help determine a manufacturing process's viability. This requires very high-speed, integrated data collection and analysis capability. For that reason image processing systems applied virtually every sector in the industrial metrology. In the past ten years the branch amount almost trebled. Presently growth amounts to approximately 6% [1].

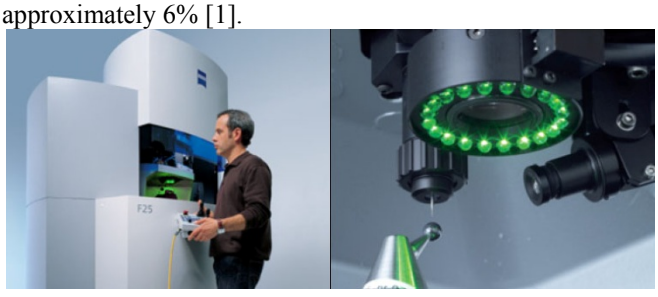

Fig. 1. Example for machine vision in a coordinate measuring machine, the Zeiss F25 [2]

Current image processing systems include integrated image analysis functions, a wide range of industrial interfaces and programmable input/output (I/O) controls. Such sophisticated features are based on the development of "smart cameras". These cameras represent an integrated image processing system in a compact housing. Smart cameras combine a digital image sensor with a built in digital signal processing devices like a DSP (digital signal processor) or a FPGA (field programmable gate array).

Since the function range and the complexity rise, fundamental understanding and the necessary technical skills in image processing and optical metrology become more and more important for engineer students. Students must learn the selection of suitable camera components as well as the programming of digital signal processors. State of the art hardware platforms offer unfortunately no possibility to arrange a comprehensive curriculum.

2. CONCEPT OF THE TEACHING SYSTEM

The new approach is to divide the basic functions of an image processing system in different stackable hardware platforms. So the students get a good overview of the mode of operation of such a system and which circuits are needed. The teaching modules guide the student from the matrix sensor up to a FPGA processing platform. The intension is to have a complete image acquisition solution which is possible to use in industrial image processing solutions and to understand how such a system works.

2.1. Working principle of image acquisition systems

A typical industrial image processing system consists of several components including illumination, lens, camera, digital or analogue interface and a computer platform with image processing software. Students have to learn to select each component for a certain task. Thereby special focus will be placed on the camera hardware.

The structure of a camera can roughly be divided into three major functions: image acquisition, optional data pre-processing and a data transfer. [Fig. 2.]

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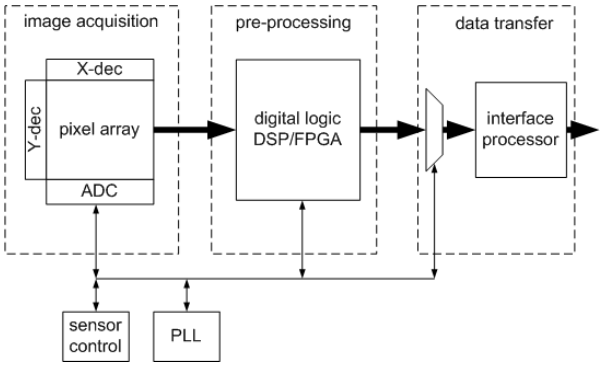

Fig. 2. Simple block diagram of a standard camera

Digital image acquisition is based on image sensors which convert photons to electrons. Today, most cameras use either a charge-coupled device (CCD) or a complementary metal–oxide–semiconductor (CMOS) sensor. Both sensor types accomplish the same task but each has unique strengths and weaknesses. Furthermore there are numerous operation characteristics like resolution, pixel size and frame rate giving advantages in different applications. The analog signals are converted to digital signals by an additional or built-in analog-to-digital-converter (ADC). As result a 8-, 10- or 12-bit wide parallel data bus, two valid data signals and the pixel clock are generated.

Data pre-processing is the second major function in a camera. In many cases, pre-processing is optionally and often only rudimentarily present for data conversion. True pre-processing on a powerful signal processor is always present in smart cameras. In most smart cameras flexible FPGAs are used. FPGAs are integrated circuits (ICs) that consist of a two dimensional array of general purpose logic blocks[1] [Fig. 3.]. Logic blocks can be configured to perform combinational functions or simple logic gates like AND and OR. [3]

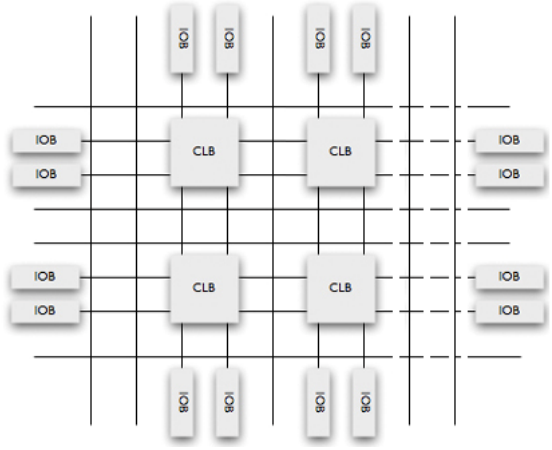

Fig. 3. FPGA block structure [4]

In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complex blocks of memory. This architecture allows the implementation of microprocessors, random access memory (RAM), read-only memory (ROM), DSP and logic functions for image pre-processing in a single chip.

The data transfer represents the concluding function block. In the last years different interfaces were established. Depending upon the application different interfaces are suitable. In most cases economical consumer interfaces like IEEE 1394 (FireWire) or Universal Serial Bus (USB) are used. Through specific requirements, like high-speed or high-resolution, highly efficient interfaces like gigabit Ethernet for machine vision (GigE Vision) or CameraLink remain the only alternatives.

Therefore it is possible to realize each functional module in a different way. From this results a huge number of hardware solutions currently available on the market.

2.2. What is the problem of actual platforms for teaching the functions of an image processing system?

Actually the trend of image sensors especially CCD/CMOS cameras is to minimize the size of the electronics and the housing [Fig. 4.]. As a result of the miniaturization it is difficult to understand how the several software tasks and the electronics in a camera work.

Fig. 4. Example of a small CCD-Camera *UI-2410-C/M* (34x32x34,4mm) [5]

Furthermore there are deficits to know on which measurement tasks the CCD/CMOS sensors are applicable, if the user does not know the specific key parameters. Additionally he does not know the advantages and the know how of camera intern pre-processing technologies. Also the required components and the component requirements for building a CCD/CMOS camera have to be considered.

If an assembled CCD/CMOS camera is used for education, for the student it is hard to understand the complete context. The camera configuration is fixed and represents only a “black box” device because main components are often unknown and unreachable for measurements. For cost reasons it is not possible for the universities to cover all configuration options with consumer cameras.

2.3. Concept of the novel multi-scalable hardware platform

The new method for the multi-scalable hardware platform is to divide the main function groups in separate working modules. So the students get several possibilities to construct their own camera system. The block diagram shown in [Fig. 2.] is therefore actually divided in three changeable toolkits. The function units are:

[1] Called configurable logic block (CLM) by Xilinx, logic cell (LC) or logic elements (LE) by Altera.

- *data acquisition function block (DAFB)* with several CCD and CMOS physical target boards,
- *data conversion and pre-processing function block (DCPFB)* with a FPGA device and Memory device
- *data transfer function block (DTFB)* with different transfer modules

The data acquisition function block contains the optoelectronic data conversion elements. That means it has to clock the CCD or the CMOS matrix sensor. In cases of a CCD solution a synchronic register transfer from the photocells into an ADC must be guaranteed.

Mostly, the information of the converted photoelectrical elements includes various (depends on the matrix sensor) black pixels around the interesting pixel elements. Eliminating the black pixels could be a task for the next block, the data conversion and pre processing function block.

The DCPFB includes all electronic requirements for a signal processing for image processing. The signal processing could be done by an FPGA or a DSP unit. Actually a FPGA unit is used for the hardware platform (Because of the multi-scalable platform it is very easy to substitute the FPGA trough a DSP depending on the electronic interconnection). So it is possible to implement parallel working software which is processed very fast. Furthermore the used DCPFP contains a SD-RAM Memory so the elements of the FPGA are not explicit used as a storage for image data. The programming interface for the FPGA depends on the supplier of the FPGA. It is mostly comfortable and supports some third party tools (for example MATLAB). With these hardware possibilities a various range of image processing can be realized. It begins with a simple data correction and ends with automatic object or pattern recognition.

After the image acquisition and the pre-processing the results must be transferred into a computer or embedded system. Transmitting data realizes the DTFB. Actual interfaces were depicted in the introduction. On a connector with a special pin out different interfaces can be connected together. So there is the possibility (depends on the pre-processing unit) to transmit all image data, pre-processed image data or a result of a calculation. For these several cases the actor has to choose a special interface depending on the required bandwidth. Actually a USB transmitting unit exists and can be used for the transfer task.

All modules are preconfigured and exist as physical component boards already. The actor has to decide which one is needed for the special task, and has a wide range of application possibilities.

2.4. Teaching modules for student training

The concepts of digital image processing are relatively difficult to impart using static mediums such as signal diagrams or filter equations. Hardware problems like the complex timing for the control of an image sensor can pose problems of proper demonstration for the lector. Similar problems arise with filter calculations. Beyond that only theoretical knowledge is imparted to the students. Practical application is missing.

These difficulties can be solved by the integration of project work in education. For a better practical orientation and for the training of interdisciplinary abilities, practically relevant image processing problems are solved by students during their education. [6] The training modules are divided in four practical courses accomplished parallel to a lecture. This ensures that the basic theory that has been taught is put into practice.

In the beginning, the students are given to solve a metrological task with the instruments of image processing. With the given conditions the students start to configure a camera with the introduced hardware platform. Using their theoretical knowledge, the students must select a sensor that meets all of the requirements.

Subsequent to the selection the integration and the signal-technical control of the sensor take place. In this module students will examine signals with an oscilloscope to appreciate the sensor control.

In the second training module students select an interface and integrate it into their hardware. Theoretical knowledge of parallel-to-serial conversion, interface standards and protocols are practically applied. The data transfer will be observed with monitoring software. At the end of this module a camera image will be presented.

The third training module deals with the implementation of digital filter algorithms based on the FPGA. After acquiring fundamental FPGA programming knowledge in the first two modules, the students will practice to solve even more complex problems. In this module the success control is accomplished at the camera image.

The last training module deals with the solution of the actual measuring problem. The configured camera will be completed with lighting and measurement setup. The students use their basics about edge detection and measurement strategies to solve the metrological task given in the first training module. Measurements are accomplished and evaluated. A practical estimation of measurement uncertainty will complete the task.

3. EVALUATION OF THE HARDWARE PLATFORM

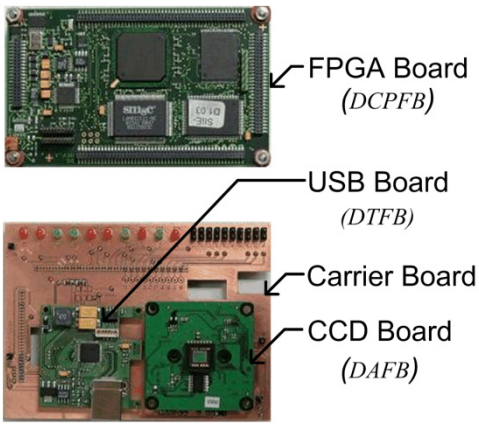

Fig. 5. Multi-scalable hardware platform with all function blocks

Based on the multi-scalable concept few physical target boards were designed and chosen. To connect all possible function blocks together it was necessary to develop a

carrier board which connects all single function modules [Fig. 5.]. Therefore, defining the pin-out for the interconnection plays an important role. It must be guaranteed that the devices can be changed without damaging and all modules for a single function are interchangeable. Beyond that it provides switches and light-emitting-diodes (LEDs) for IO control.

For the DAFB a development board with a Xilinx Spartan IIE was selected. The programmable-logic device features up to 300.000 system gates and can be programmed using a JTAG interface. Additionally the board provide fast Static Random Access Memory (SRAM) as buffer memory, Flash RAM for boot loader and low-level communication interfaces.

The first realized module for the DCPFB is a universal serial bus 2.0 (USB) interface. A configurable Cypress USB controller enables data transfer rates of up to 480 Mbits/s which allows data handling between the hardware platform and an image processing unit. In addition, the FPGA Development Board (DAFB) includes a triple 10 Bit video digital-to-analog-converter (DAC) from Texas Instruments. These IC permit a software related configuration to produce the complete range of analog component video and PC graphics (VESA) formats.

For image acquisition several modules with CCD and CMOS sensors were developed. Primarily 1/3 inch CCD sensors from Sony used to ensure on the one hand the acquisition of qualitatively high-quality pictures and to hold on the other hand the price of the sensors in an acceptable range. In order to cover different applications, sensors for high-speed and high-resolution are available.

4. RESULTS AND DISCUSSION

For a first practical validation of the training concept the modules were combined into an one-day training workshop with five students. In order to become fair the tightened schedule and the complex topic, the modules, departing from the concept, were shortened and changed over slightly.

4.1 Validation of the teaching system

On the basis of the sensor choice, the students accomplished oscilloscope measurements of the sensor signals as well as of the digital signals of the sensor board (DAFB). During the Workshop a CCD sensor was used. Comparatively to the datasheet thereby timings of the digital signals were taken up. Parallel to the measurements the theoretical bases of the different readout methods were repeated.

Differently than intended in the concept, in the second module within the FPGA a simple bit filter was realized (originally module three). Because of the complex task of programming, it was decided to omit the realization of a matrix filter. Instead the bases of the VHDL (Very High Speed Hardware Description Language) programming were obtained. Starting point for the workshop was an incomplete VHDL project. Throughout the training, the students completed the project by generating some of the modules from scratch and by completing others from existing files. The focus of this module lays on converting taken up timings to synchronize on the digital data stream. For verification the data stream channeled through the FPGA was inverted.

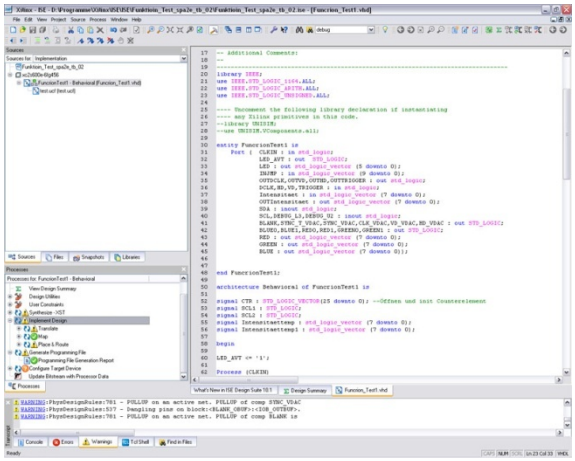

Fig. 6. Xilinx ISE™ Design Suite with unfinished modules

However the realization of the FPGA design flow in the final course is not specified yet. Possible software solutions are the Xilinx Integrated Software Environment (ISE™) or the graphical programming with MATLAB/Simulink. The Xilinx ISE™ has the advantage that the standard design flow, initiating with the design entry over synthesis, place and route up to programming is accomplished. The disadvantage is the strong restriction on the Xilinx design tools and the overall complex programming effort. MATLAB/Simulink offers the possibility to comprehend and program the algorithms themselves relatively fast. However the essential FPGA programming remains quite superficial. During the Workshops the Xilinx ISE™ was used. For finally decision a second workshop with Matlab programming is planned.

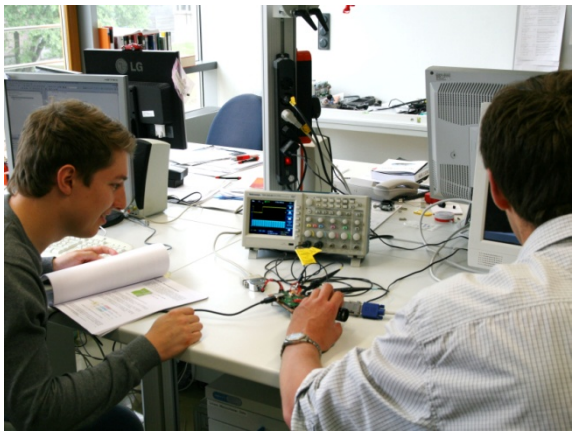

Fig. 7. Student during practice workshop in Ilmenau

In the third module the complexity was increased by implementation an interface control. In the workshop the control of the video DAC should take place, to generate a RGB (red, green, blue) analog component video output for a VGA (Video Graphics Array) interface. RGB component video requires synchronization signals parallel to the video

signals. These blanking and synchronization signals are generated by toggling appropriate pins on the video DAC [7]. The results could be examined on the one hand with the oscilloscope and on the other hand directly by the VGA output at the computer screen.

Since the multi-scalable hardware platform was not embedded yet into a measuring software, module four was realized independently of the platform on an existing system. Thereby the structure of an existing practical course was adopted. The students accomplished transmitted light measurement of a motor core lamination.

4.2 Evaluation of the student's opinions on the workshop

The students were interviewed at the end of the workshop, regarding their estimate for the success in learning of the course. According to the opinions of the students the work with FPGA represents a very interesting in addition, very complex area of application. A combination of theory and practice makes it easier to understand the individual work procedures of the FPGA design flow. In addition, it showed that a practical course can only offer a short introduction to such a wide topic. However, it must consider the number of participants is not representativ.

5. CONCLUSIONS AND OUTLOOK

The necessary training of image processing abilities can be integrated into the education at universities by practical work with a transparent hardware. A multi-scalable hardware platform was developed to bring theory and practice closer together. For entering in a direct application a working solution for all defined function blocks actually exist. With the available hardware components students are able to configure and implement a smart camera for different measurement tasks.

In order to extend the multi-scalability of the hardware platform further modules are planned. Primarily there are efforts to implement more interfaces. Accordingly modules for GigE Vision, DVI and other standard interfaces must be developed. The next main innovation will be the development of a DCPFB on basis of a DSP. Beyond that there would be the possibility to control lighting components and actuators with extension modules.

In the course of the completion of the training environment the transfer takes place into a parallel lecture where the theoretical bases are taught. The lecture with attached practical course will be offered in the consecutive course "Optronik" at the Ilmenau University of Technology. "Optronik" is a cross section science, which unites the technical disciplines optics, electronics, mechanics and information technology to a new discipline.

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